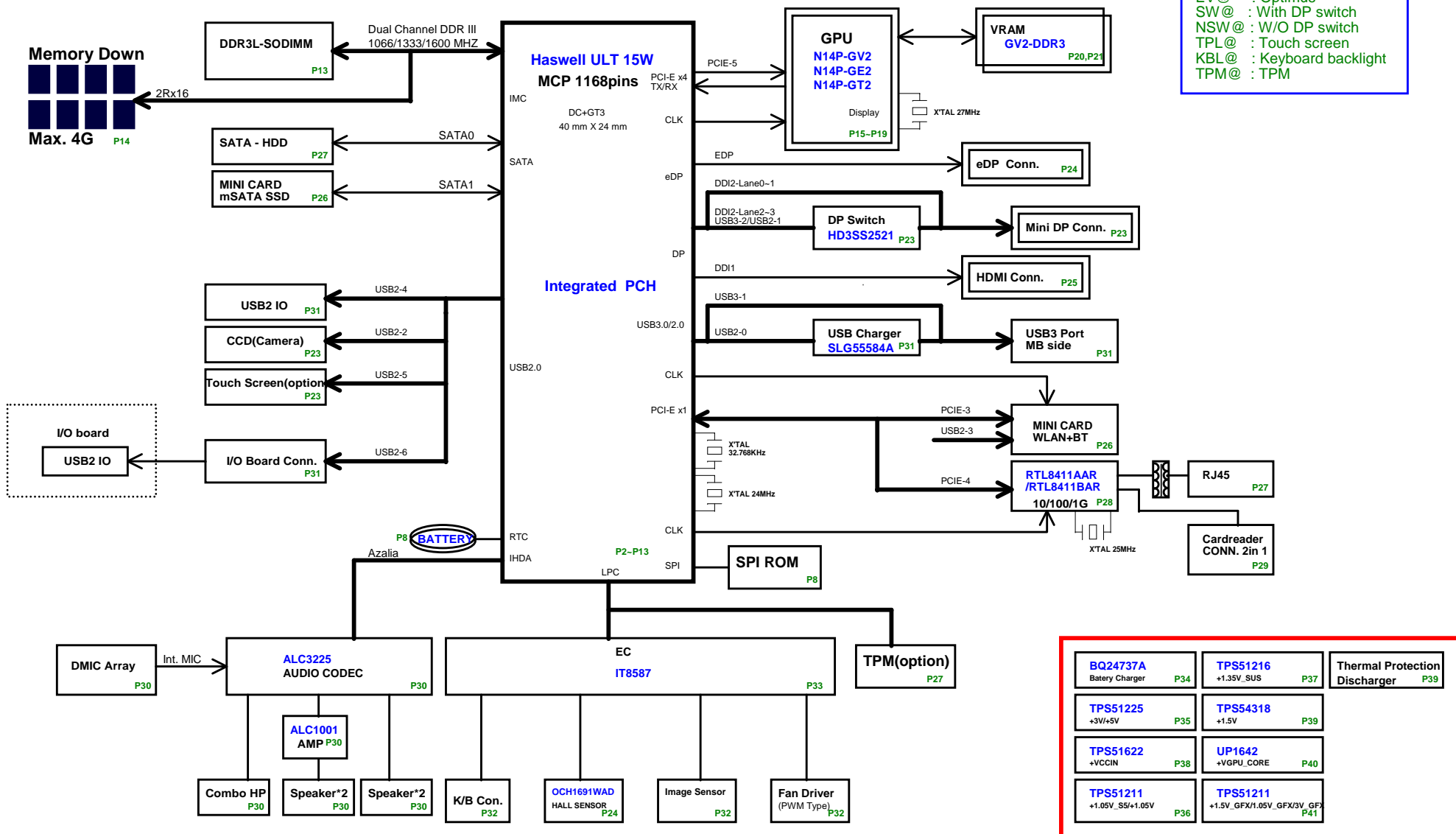


ZRQ_GDDR3 SHB ULT SYSTEM BLOCK DIAGRAM

BOM

01

IV@ : iGPU
EV@ : Optimus
SW@ : With DP switch
NSW@ : W/O DP switch
TPL@ : Touch screen
KBL@ : Keyboard backlight
TPM@ : TPM



BQ24737A Battery Charger P34	TPS51216 +1.35V_SUS P37	Thermal Protection Discharger P39
TPS51225 +3V/+5V P35	TPS54318 +1.5V P39	
TPS51622 +VCCIN P38	UP1642 +VGPU_CORE P40	
TPS51211 +1.05V_SS/+1.05V P36	TPS51211 +1.5V_GFX/1.05V_GFX/3V_GFX P41	

Haswell ULT (DISPLAY,eDP)

02

HDMI

Mini DP

25 INT_HDMITX2N
25 INT_HDMITX2P
25 INT_HDMITX1N
25 INT_HDMITX1P
25 INT_HDMITX0N
25 INT_HDMITX0P
25 INT_HDMICLK-
25 INT_HDMICLK+

C54 DDI1_TXN0
C55 DDI1_TXP0
B58 DDI1_TXN1
C58 DDI1_TXP1
B55 DDI1_TXN2
A55 DDI1_TXP2
A57 DDI1_TXN3
B57 DDI1_TXP3

23 DP2_TXN0
23 DP2_TXP0
23 DP2_TXN1
23 DP2_TXP1
23 DP2_TXN2
23 DP2_TXP2
23 DP2_TXN3
23 DP2_TXP3

C51 DDI2_TXN0
C50 DDI2_TXP0
C53 DDI2_TXN1
B54 DDI2_TXP1
C49 DDI2_TXN2
B50 DDI2_TXP2
A53 DDI2_TXN3
B53 DDI2_TXP3

EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1
EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3

EDP_AUXN
EDP_AUXP
EDP_RCOMP
EDP_DISP_UTIL

C45 EDP_TXN0
B46 EDP_TXP0
A47 EDP_TXN1
B47 EDP_TXP1
C47 EDP_TXN2
C46 EDP_TXP2
A49 EDP_TXN3
B49 EDP_TXP3
A45 EDP_AUXN
B45 EDP_AUXP

D20 EDP_RCOMP
A43 DP_UTIL

eDP Panel

eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils

24 PCH_BRIGHT
24 PCH_BLON
24 PCH_VDDEN

PCH_BRIGHT
PCH_BLON
PCH_VDDEN

B8
A9
C6

EDP_BKLCCTL
EDP_BKLEN
EDP_VDDEN

eDP SIDE BAND

DDPB_CTRLCLK
DDPB_CTRLDATA
DDPC_CTRLCLK
DDPC_CTRLDATA

B9 HDMI_DDCCLK_SW
C9 HDMI_DDCDATA_SW
D9 DDPC_CTRLCLK
D11 DDPC_CTRLDAT

TP46

PCI_PIRQA#
PCI_PIRQB#
PCI_PIRQC#
PCI_PIRQD#
PCI_PME#

U6
P4
N4
N2
AD4

PIRQA/GPIO77
PIRQB/GPIO78
PIRQC/GPIO79
PIRQD/GPIO80
PME

+3V
+3V
+3V
+3V
+3V_S5
PCIe

DDPB_AUXN
DDPC_AUXN
DDPB_AUXP
DDPC_AUXP

C5
B6
B5
A6

INT_DP_AUXDN
INT_DP_AUXDP

TP_INT_PCH
DDPC_CTRLCLK
DDPC_CTRLDAT

DDPB/C_CTRLDATA has an iPD 20K,
When PU at rising edge of
PCH_PWROK, the DDI port will
be detected

24 TP_INT_PCH
10 BOARD_ID4
10 BOARD_ID1
10,32 BOARD_ID2

DGPU_SELECT#
BOARD_ID4
BOARD_ID1
BOARD_ID2

U7
L1
L3
R5
L4

GPI055
GPI052
GPI054
GPI051
GPI053

+3V
+3V
+3V
+3V
+3V

DDPB_HPD
DDPC_HPD
EDP_HPD

C8
A8
D6

INT_HDMI_HPD
DP_HPD_Q
EDP_HPD

R806
100K_4

PCI_PIRQA#
PCI_PIRQB#
PCI_PIRQC#
PCI_PIRQD#
DGPU_SELECT#

R160
R635
R623
R617
R601

TP_INT_PCH
DDPC_CTRLCLK
DDPC_CTRLDAT

R175
R576
R575

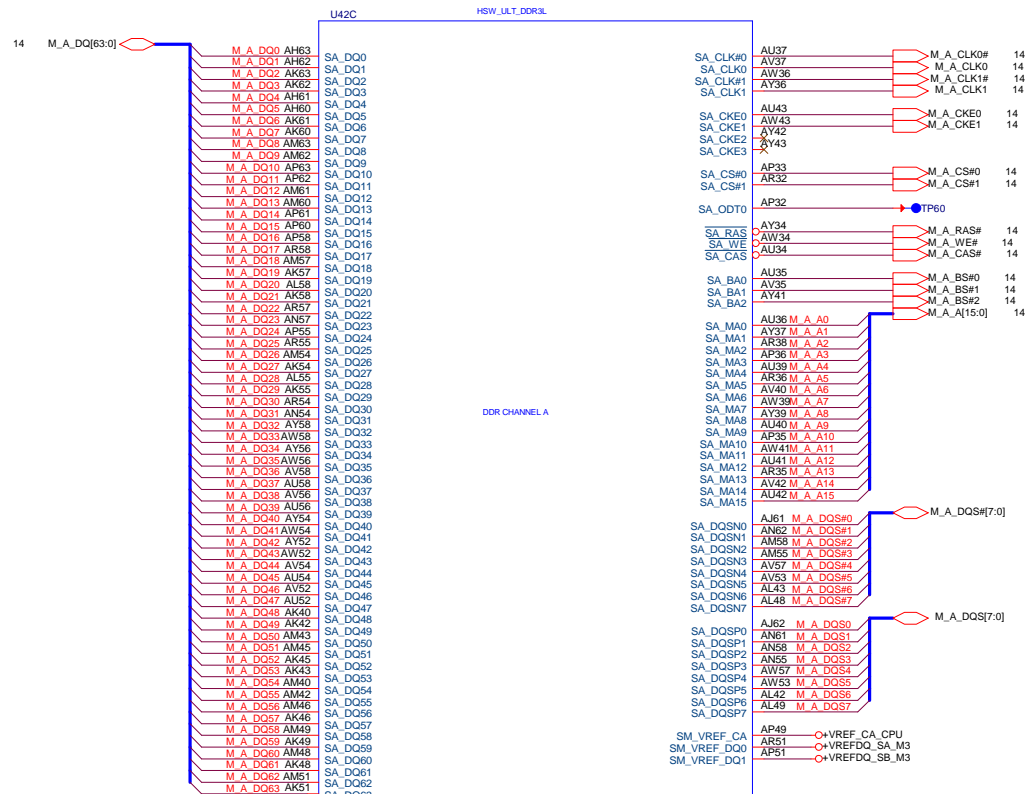


Quanta Computer Inc.

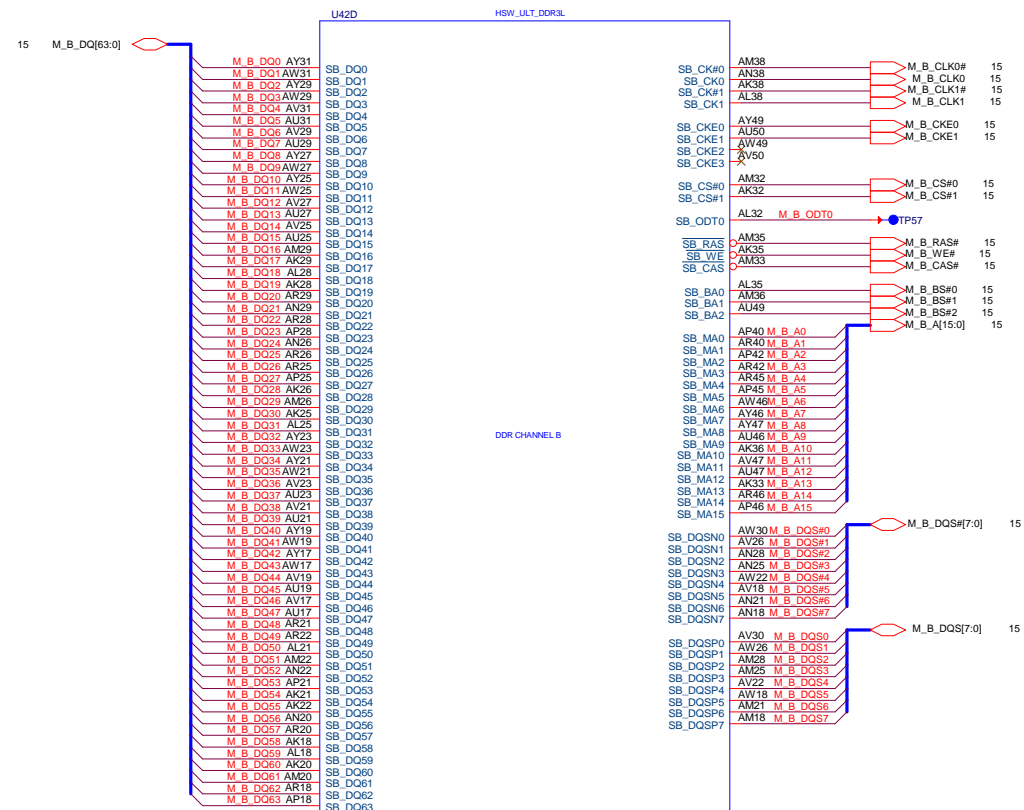
PROJECT : ZRQ

Size	Document Number	Rev
	Haswell 3/5 (DDI/eDP)	3A
Date:	Friday, April 12, 2013	Sheet 2 of 47

Haswell ULT (DDR3L)



Haswell Processor (DDR3)

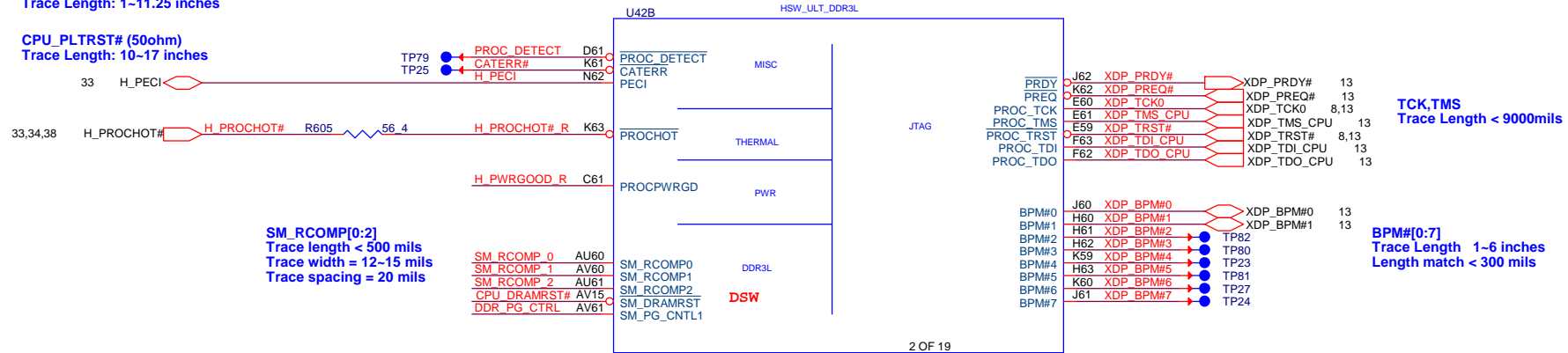


Haswell ULT (SIDE BAND)

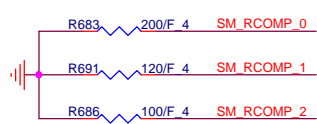
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

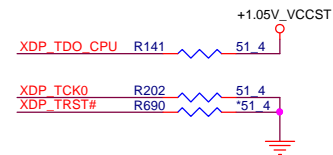
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



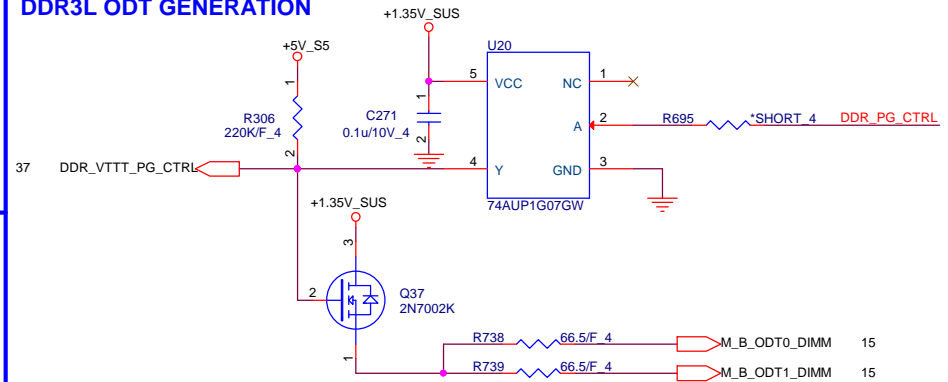
DRAM COMP



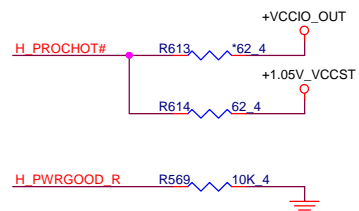
XDP PU/PD



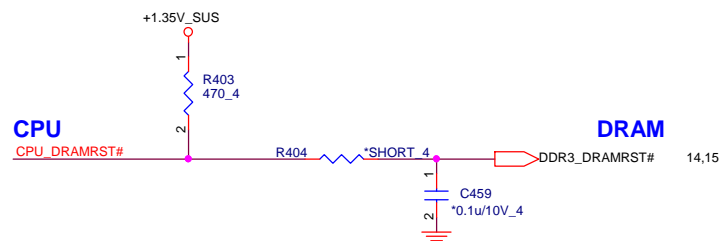
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



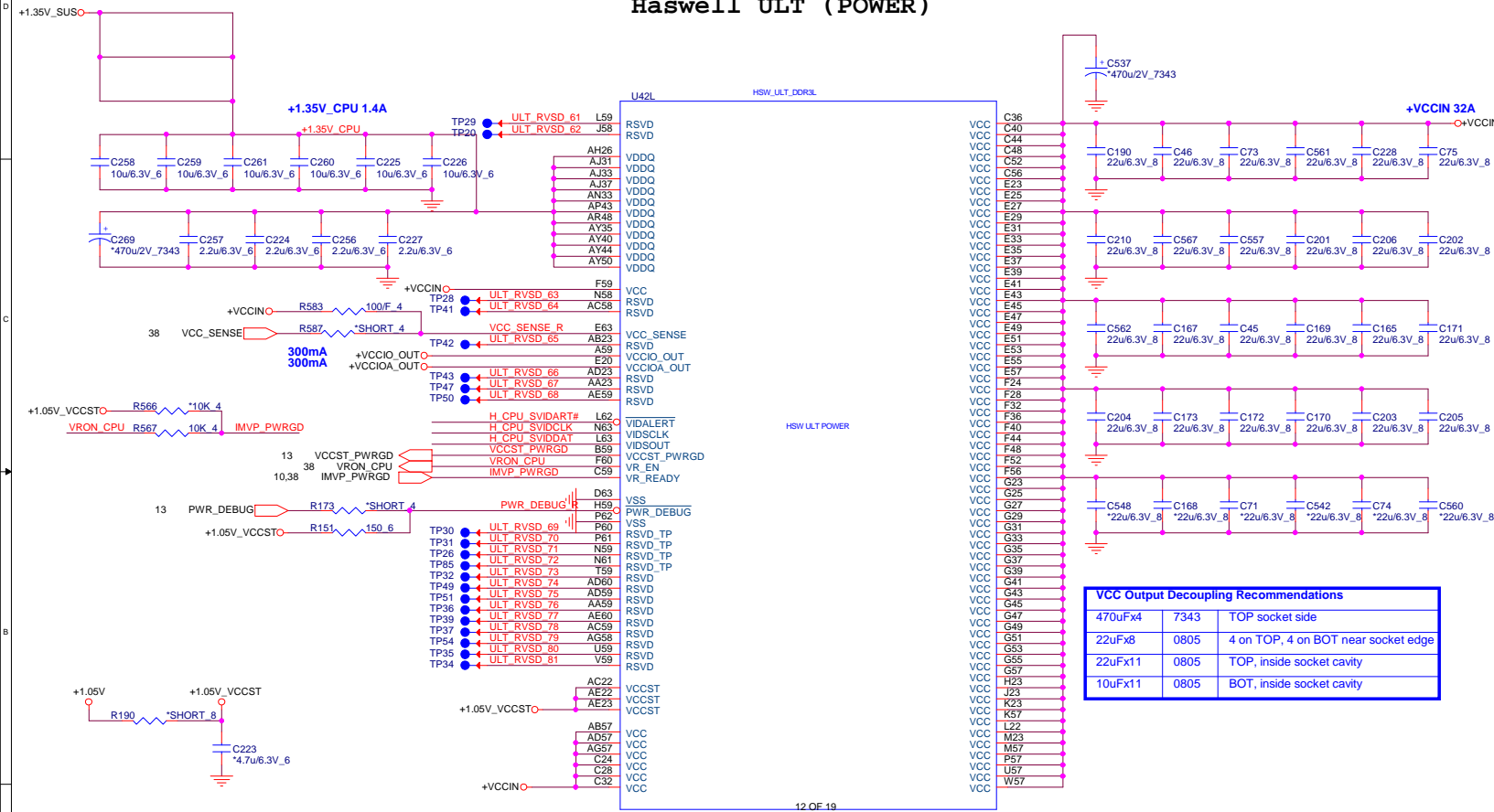
Quanta Computer Inc.

PROJECT : ZRQ

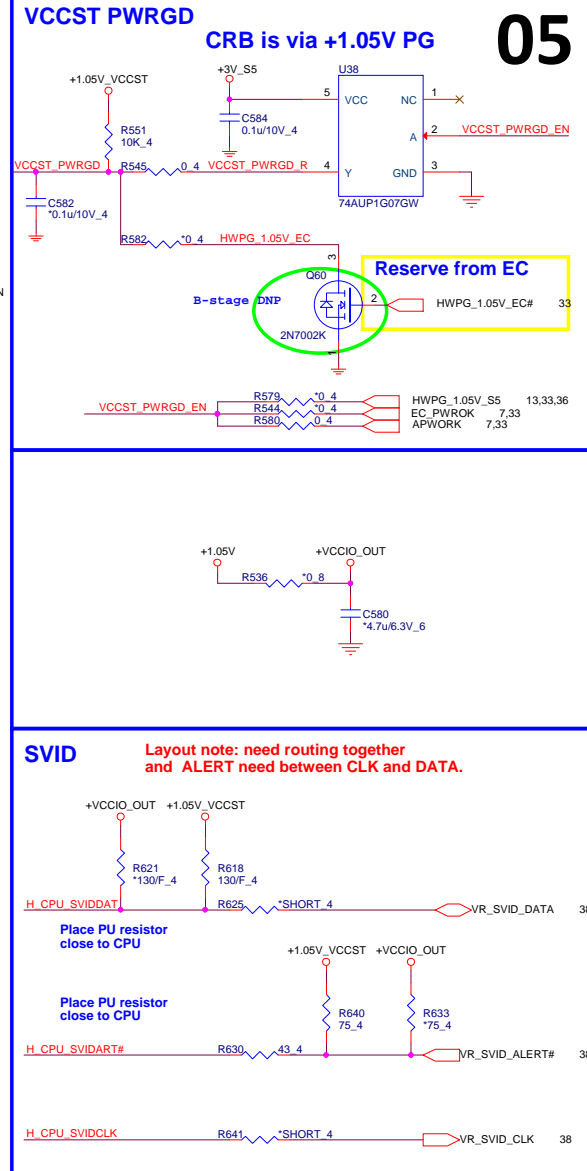
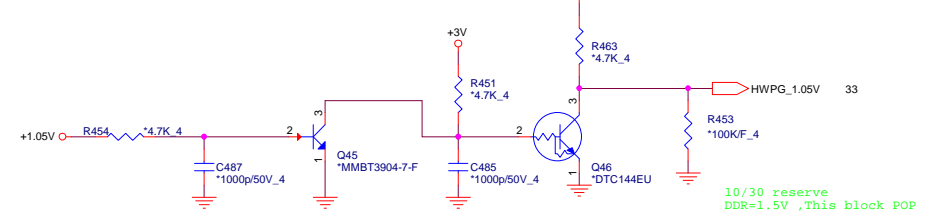
Size	Document Number	Rev
	Haswell 1/5 (PEG/DM/FDI)	3A
Date:	Friday, April 12, 2013	Sheet 4 of 47

VDDQ Output Decoupling Recommendations			
330uFx2	7343	BOT socket side	
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity	
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity	

Haswell ULT (POWER)

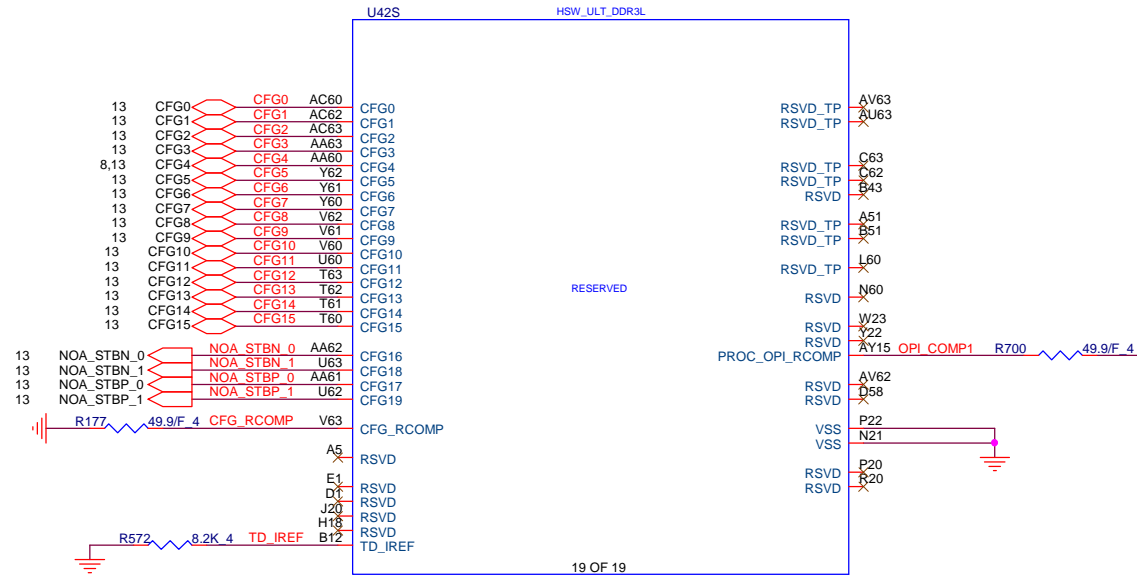


HWPG_1.05V for DDR=1.5V



Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R203 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R184 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R192 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R171 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R172 *1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R183 *1K 4

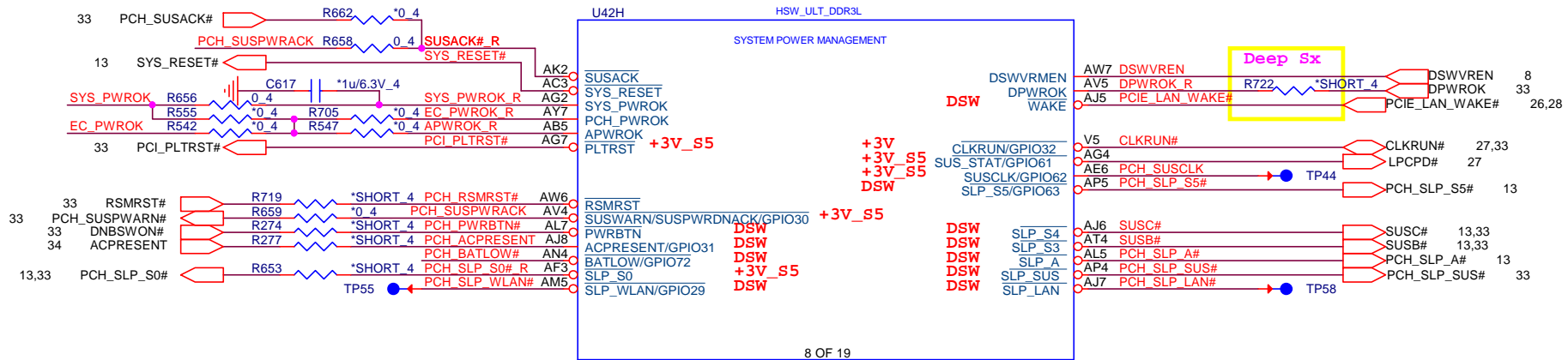


Quanta Computer Inc.

PROJECT : ZRQ

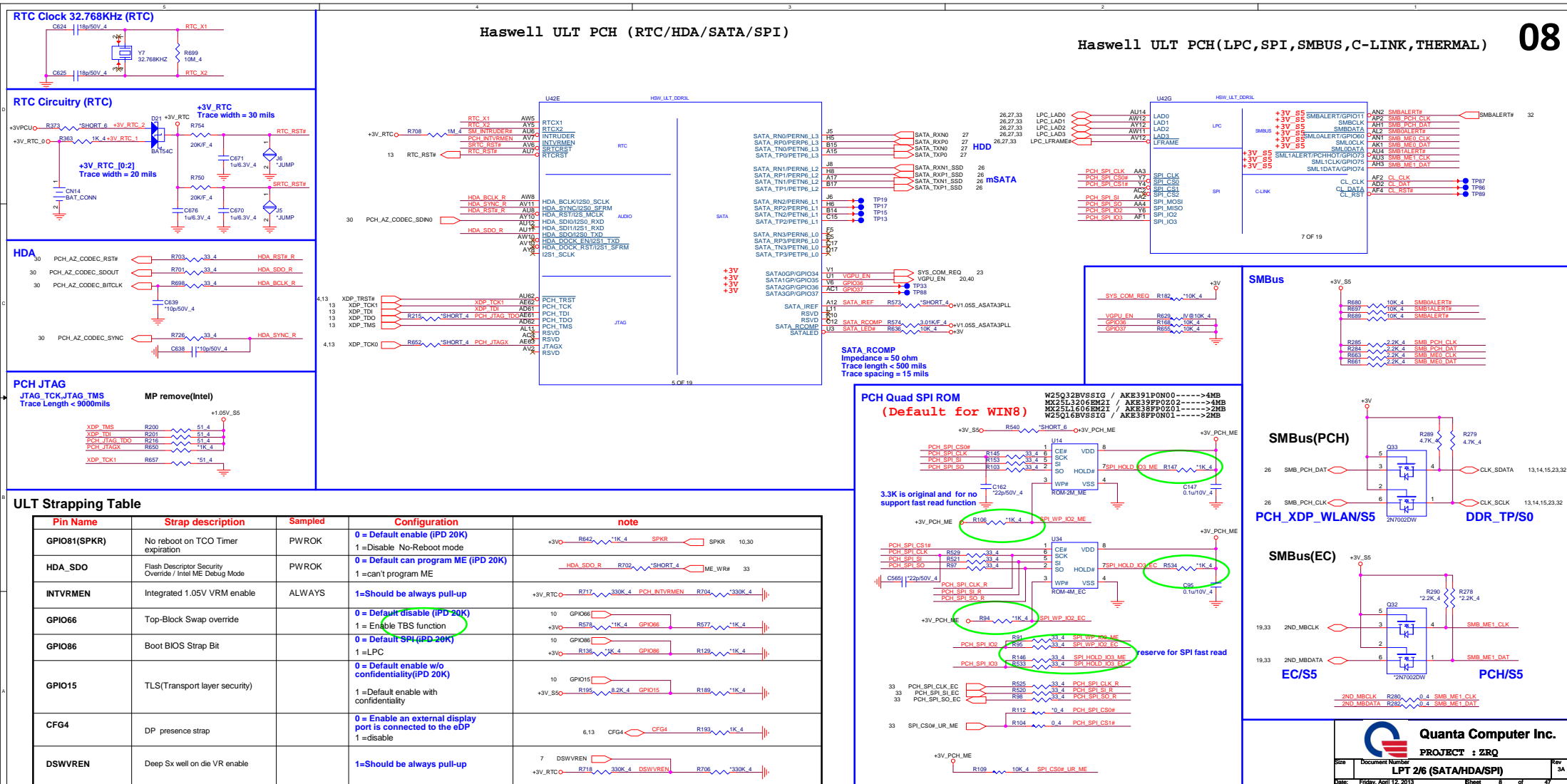
Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	3A
Date: Friday, April 12, 2013	Sheet	6 of 47

Haswell ULT PCH (PM)

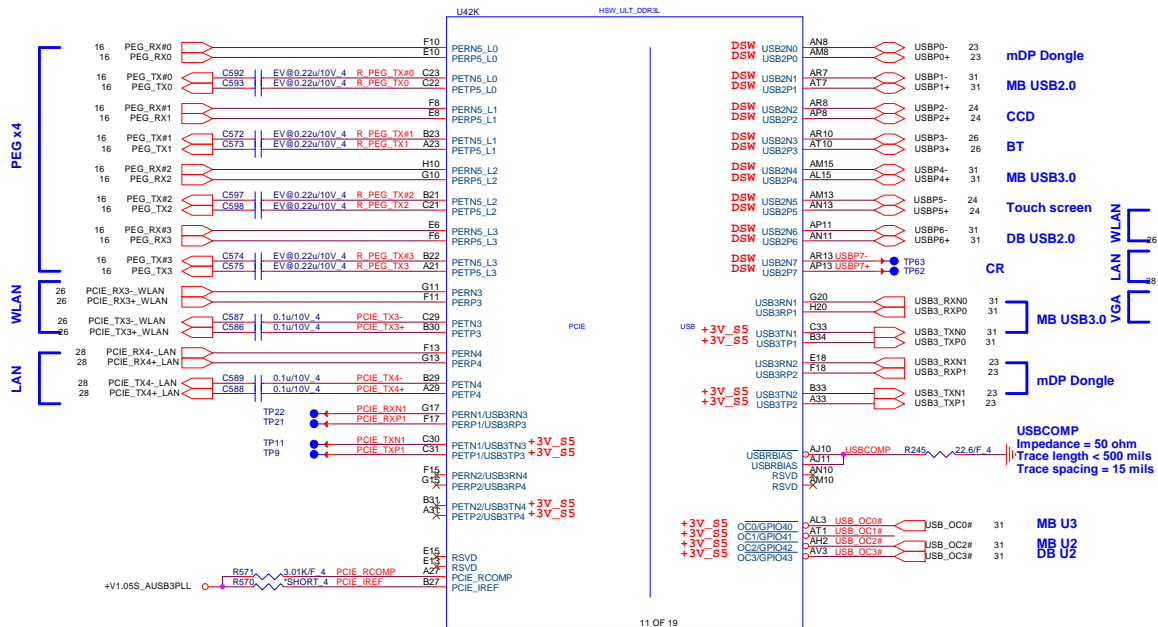


Haswell ULT PCH (RTC/HDA/SATA/SPI)

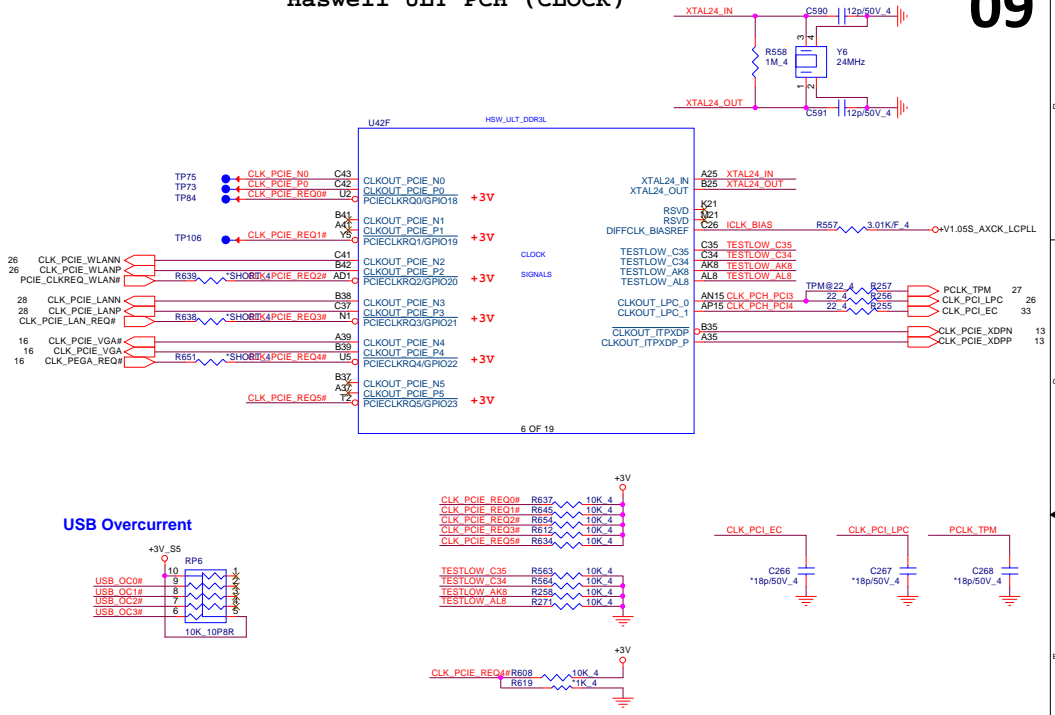
Haswell ULT PCH(LPC, SPI, SMBUS, C-LINK, THERMAL)




```
Haswell ULT PCH (PCIE,USB3.0,USB2.0)
```



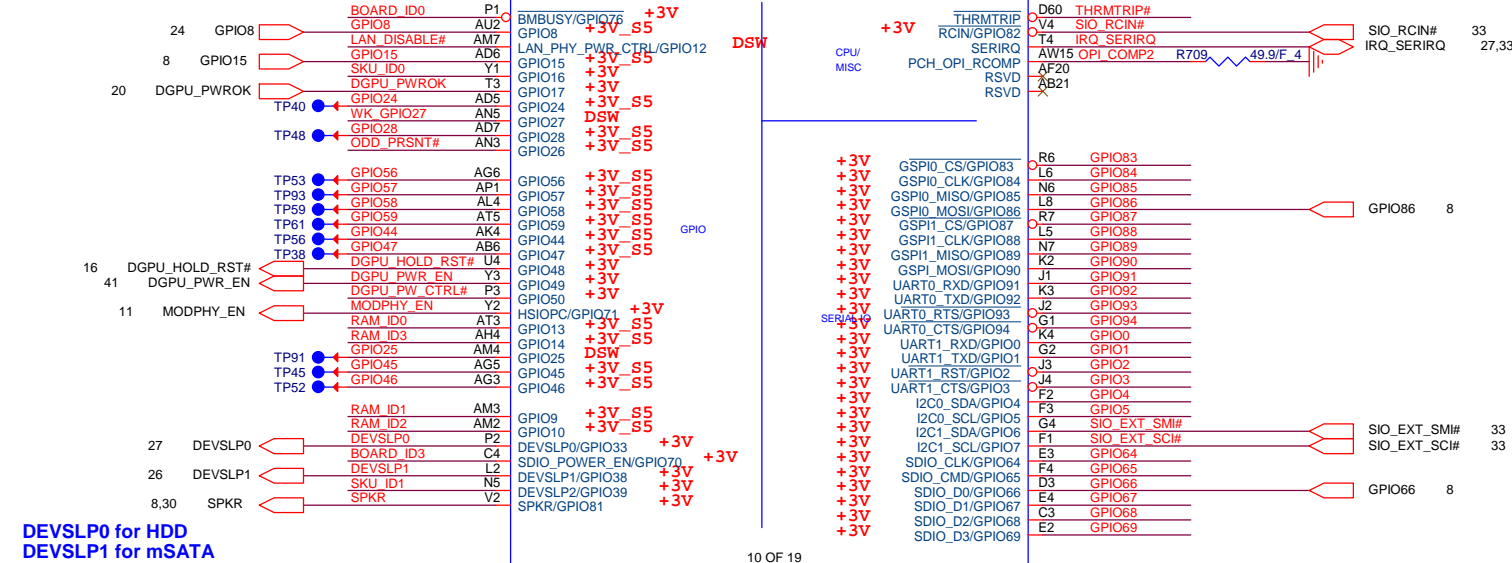
```
Haswell ULT PCH (CLOCK)
```



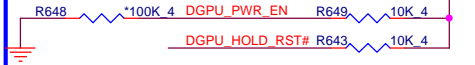
Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

10

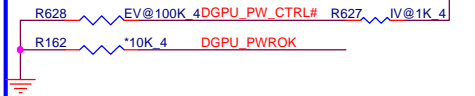
	High	Low
GPIO8	No touch panel	Touch panel



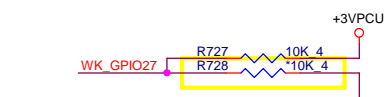
IRQ_SERIRQ	R159	10K 4
DEVSLP0	R169	10K 4
DEVSLP1	R611	10K 4
SIO_RCIN#	R187	10K 4
SIO_EXT_SM#	R135	10K 4
SIO_EXT_SCI#	R131	10K 4
GPIO83	R206	10K 4
GPIO84	R150	10K 4
GPIO85	R207	10K 4
GPIO87	R152	10K 4
GPIO88	R208	10K 4
GPIO89	R205	10K 4
GPIO90	R597	10K 4
GPIO91	R594	10K 4
GPIO92	R209	10K 4
GPIO93	R590	10K 4
GPIO94	R588	10K 4
GPIO1	R589	10K 4
GPIO2	R595	10K 4
GPIO3	R592	10K 4
GPIO4	R585	10K 4
GPIO5	R586	10K 4
GPIO64	R584	10K 4
GPIO65	R134	10K 4
GPIO67	R130	10K 4
GPIO68	R128	10K 4
GPIO69	R581	10K 4



high	UMA Only
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)

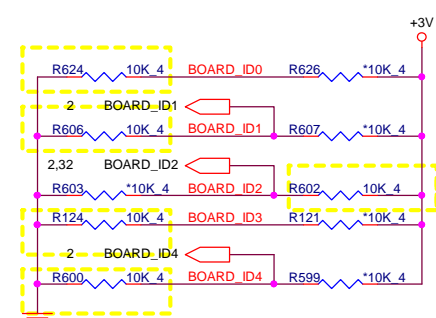


LAN_DISABLE#	R260	10K 4
ODD_PRSTNT#	R679	10K 4
GPIO8	R250	10K 4



GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

Board ID



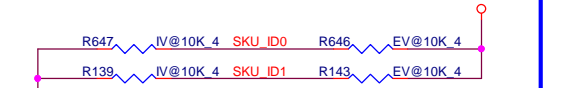
	Low	High
BOARD_ID0	DDR3	GDDR5
BOARD_ID1	Enable on board memory	Disable on board memory
BOARD_ID2	Pin8 of SYNAPTICS and ELAN are NC pin. BIOS maybe will use EEPROM detection. Default is pull high.	
BOARD_ID3	Reserved (Default)	Reserved
BOARD_ID4	Reserved (Default)	Reserved

RAM ID



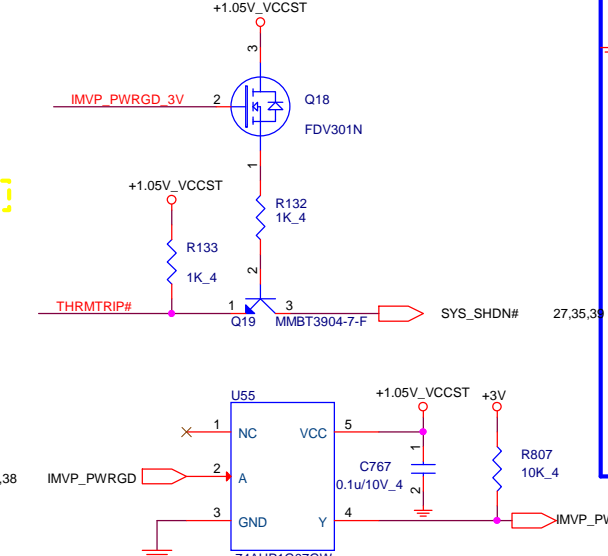
Vender	RAM_ID	Q PN	Mfr. PN	Freq.
Hynix	0000	AKD5JGETW04	H5TC4G63AFR-PRBA	1600MHz
Elpida	0001	AKD5JGST400	EDJ4216EBBG-DJ-F	1333MHz
Elpida	0010	AKD5JGST404	EDJ4216EFBG-GN-F	1600MHz

SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

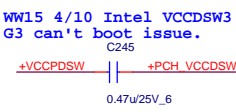
CPU thermal trip



Quanta Computer Inc.

PROJECT : ZRQ

Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	3A
Date:	Friday, April 12, 2013	Sheet 10 of 47



The schematic diagram shows the USB3 PLL circuit. The main component is the TPS22965DSGR (U40). The circuit is powered by +1.05V_S5 and +5V_S5. The output is +V1.05DX_MODPHY. The circuit includes several resistors (R604, R185, R188, R560) and capacitors (C601, C602, C607, C608). The circuit is labeled 'MODPHY_EN' and 'MODPHY'.

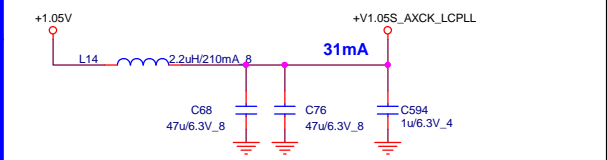
11mA

+3V_S5 +V3.3DX_1.5DX_1.8DX_AUDIO

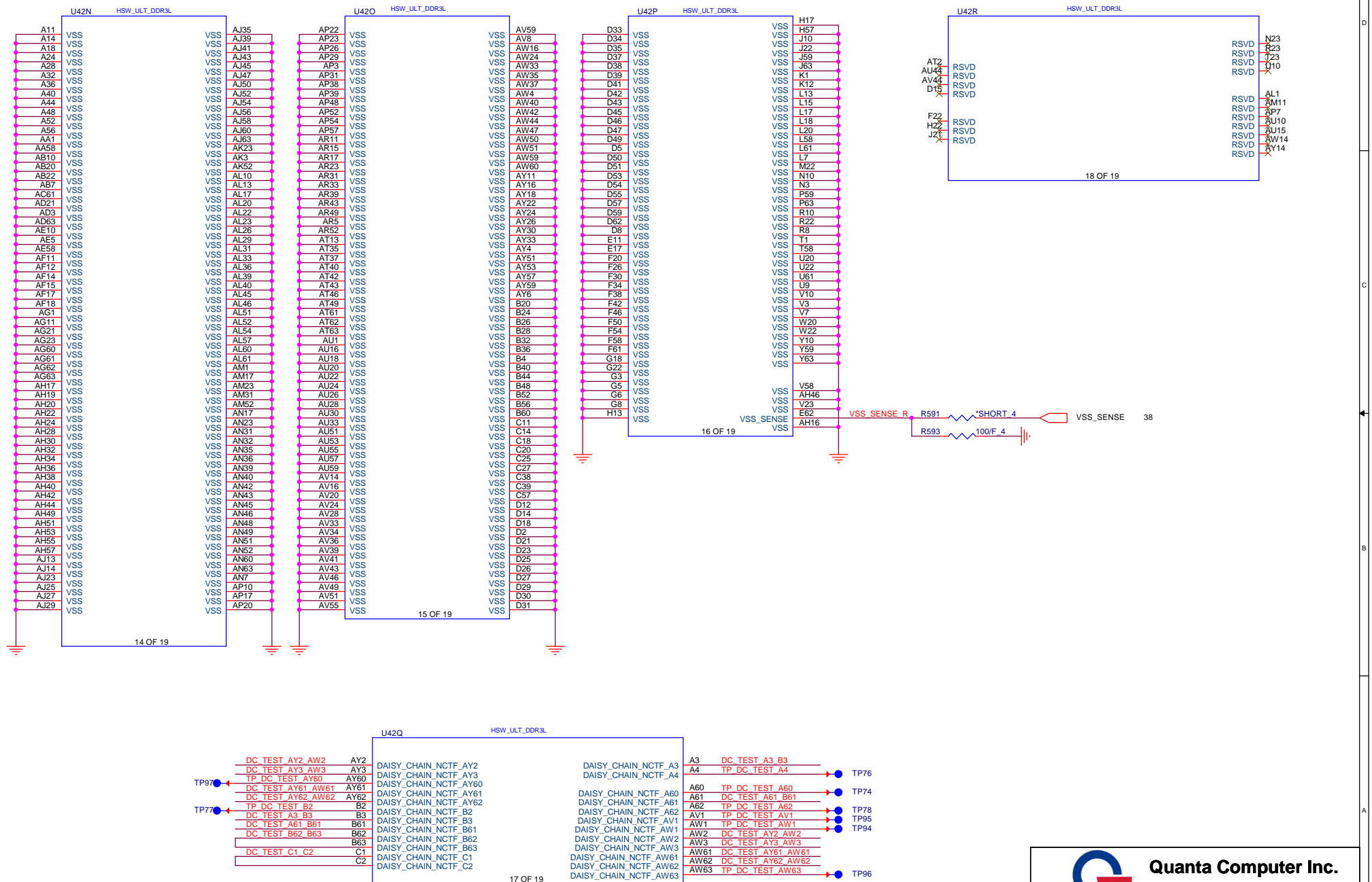
R252 *SHORT 6

C234 0.1u/10V_4

Place close to ball



Haswell ULT (GND)



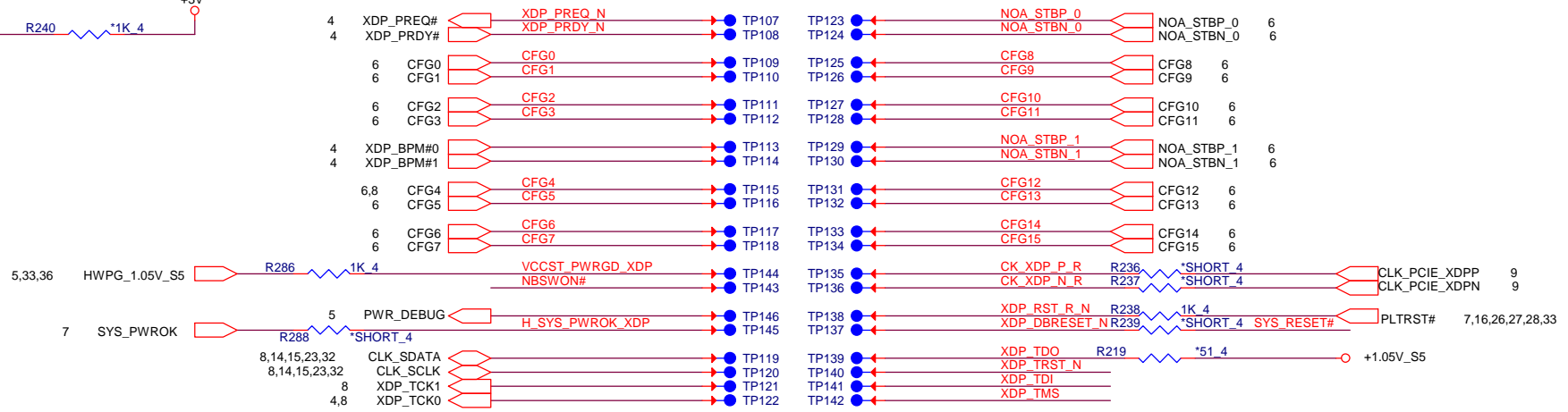
Quanta Computer Inc.

PROJECT : ZRQ

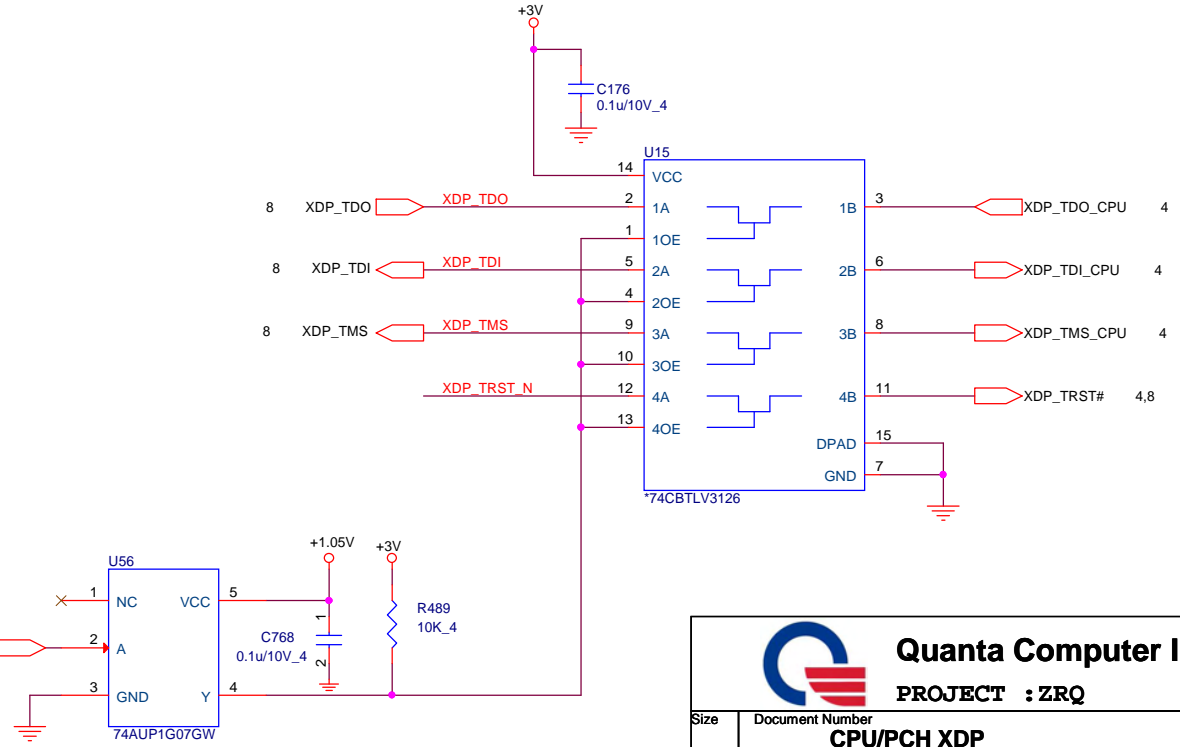
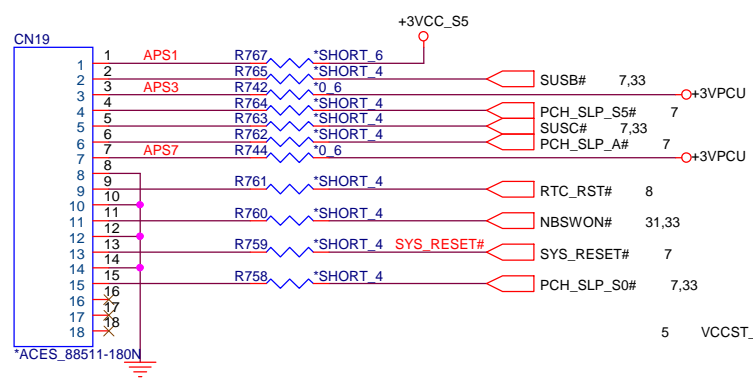
Size	Document Number	Rev
	LPT 6/6 (GND)	3A
Date:	Friday, April 12, 2013	Sheet 12 of 47

H_SYS_PWROK_XDP R287 *1K 4 +3V_S5

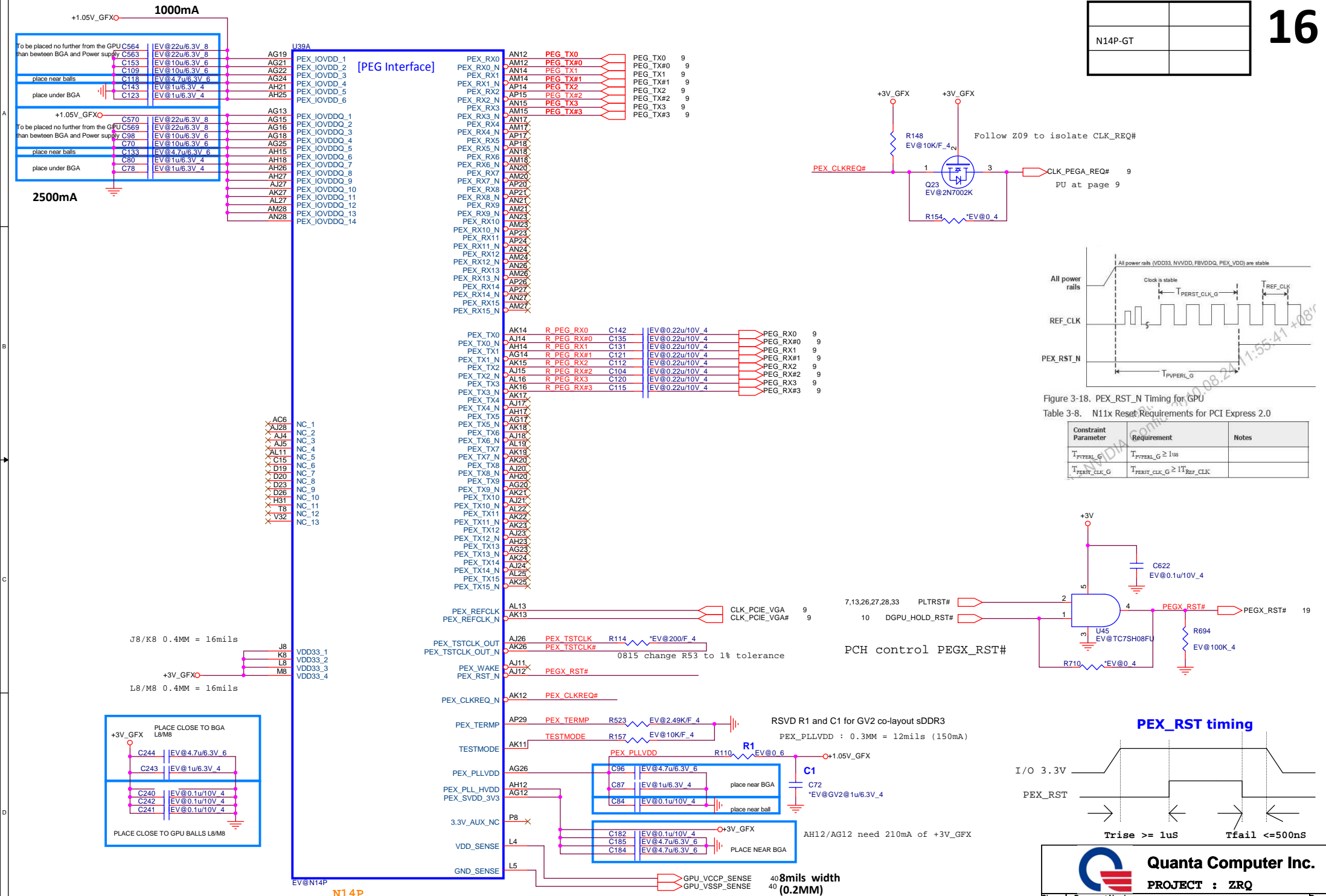
XDP_DBRESET_N R240 *1K 4 +3V

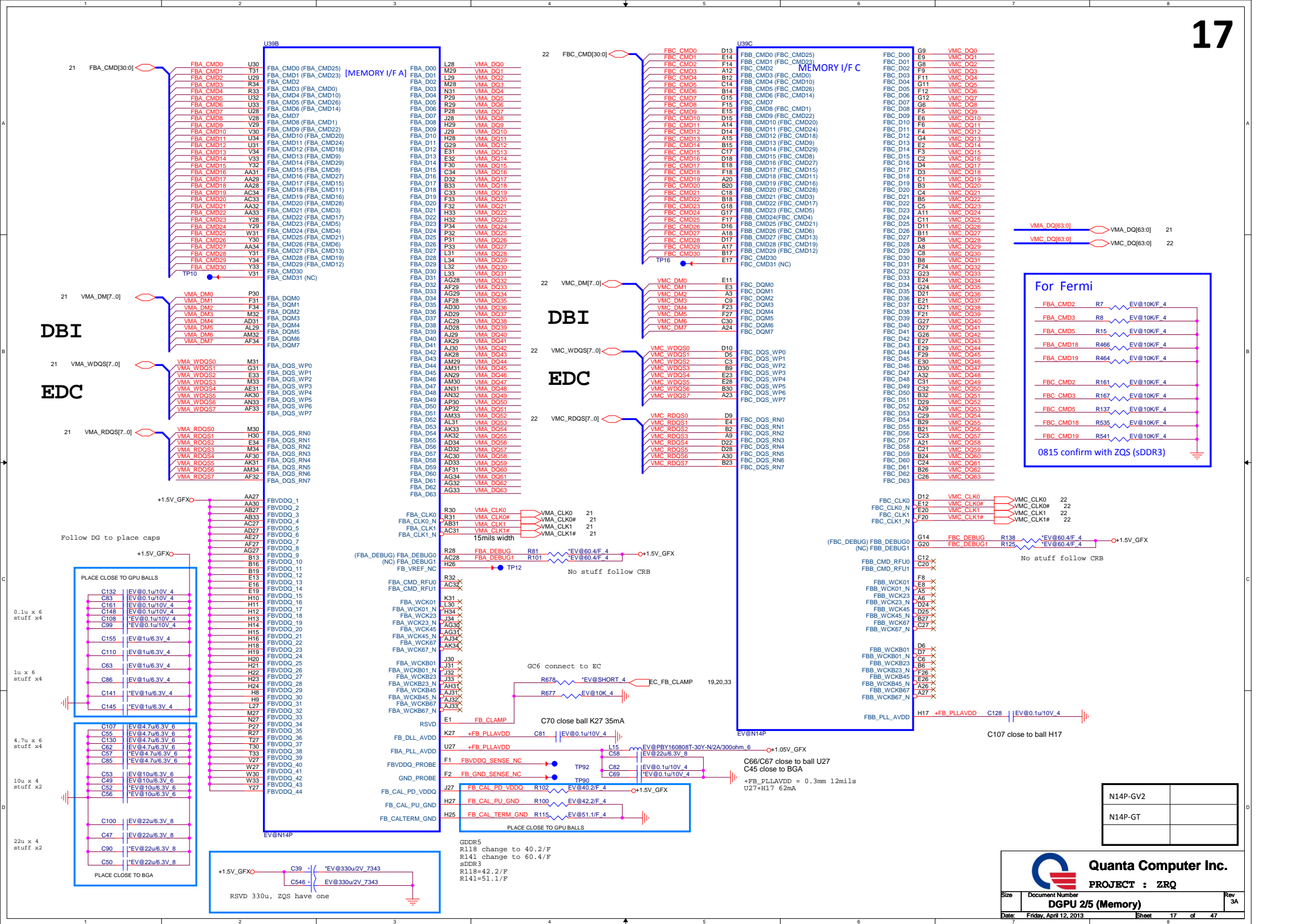


APS

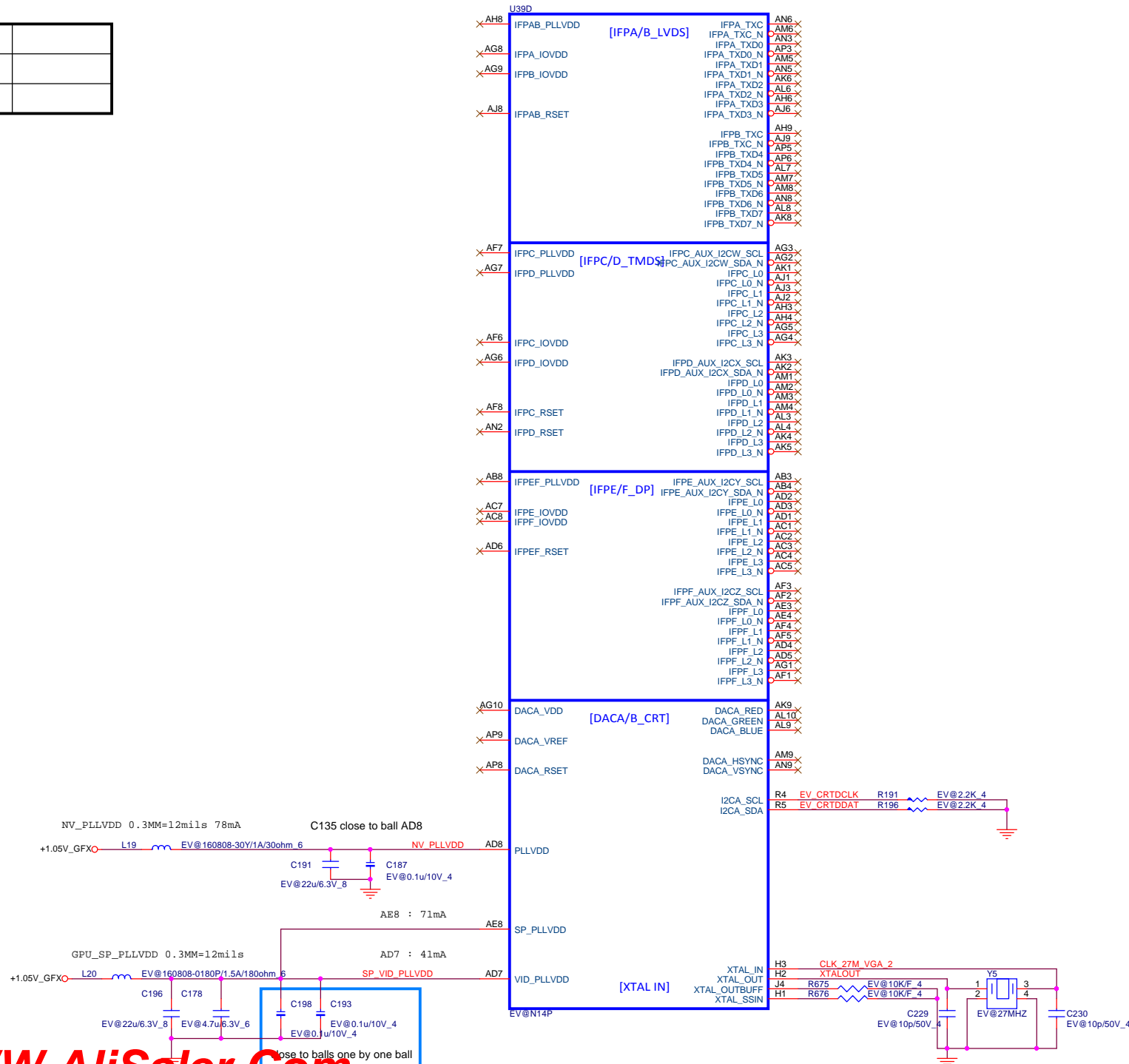








N14P-GV2	
N14P-GT	



Logical Strap Bit Mapping		
	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

STRAP3
Optimus ----> 4.99k PD
Discrete only ----> 15K PD

Resistor P/N

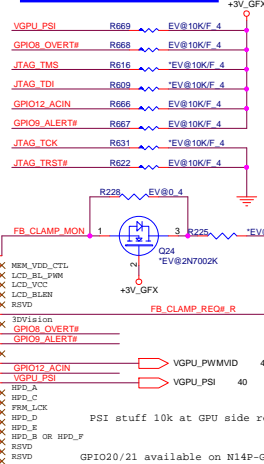
4.99K----	CS24992FB26
10K ---->	CS31002FB26
15K ---->	CS31502FB26
20K ---->	CS32002FB29
24.9K----	CS32492FB16
30.1K----	CS33012FB18
34.8K----	CS33482FB22
45.3K----	CS34532FB28

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	100
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	001
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	000
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	010
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD03	011

	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P_GV	L_10K	H_4.99K	H_4.99K	H_45.3K	L_45.3K	L_15K	L_4.99K	L_45.3K
N14P_GE	L_10K	L_10K	L_10K	H_10K	H_10K	L_10K	L_10K	L_10K
N14P_GT	L_10K	H_4.99K	L_15K	H_45.3K	L_4.99K	L_24.9K	L_4.99K	L_45.3K

19

```
N14P-GV2 ES device ID=0x12AD
1.ROM_SCLK =15K pull down
2.STRAP2= 30k pull high
3.STRAP4=10K pull down
//For N14P-GV2 ES
```



STRAP0 J2 STRAP0
 STRAP1 J7 STRAP1
 STRAP2 J6 STRAP2
 STRAP3 J5 STRAP3
 STRAP4 J3 STRAP4
 R3
 574 EV@40.2K/F 4 J1 MULTIST
 form EC EV@N14P

[MISC2_ROM]
ROM
ROM
F
R

_REF_GND


BUR

H4 ROM SCLK
H6 R178 EV@10K_4 +3V_GFX
H5 ROM SI
H7 ROM SO

L2 R670 *EV@10K.4

L3 CEC is NC for GK107

from EC

3  dGPU_ALT# 33

```

dGPU_ALT# = EC cor
EV@0_4 PEGX_RST#

```

GPIO12 HW throttle
over power protect dGPU on

+3V_GFXO

Diagram of a U3 gate. A blue arc connects two red lines. The top red line is labeled '4' and the bottom red line is labeled '2'. The gate is labeled 'U3'.

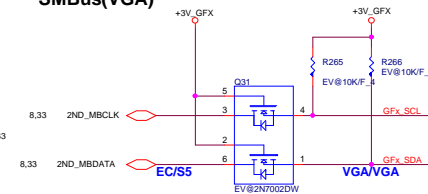
*EV@MC74VHC1G08DFT2G RSVD VGP

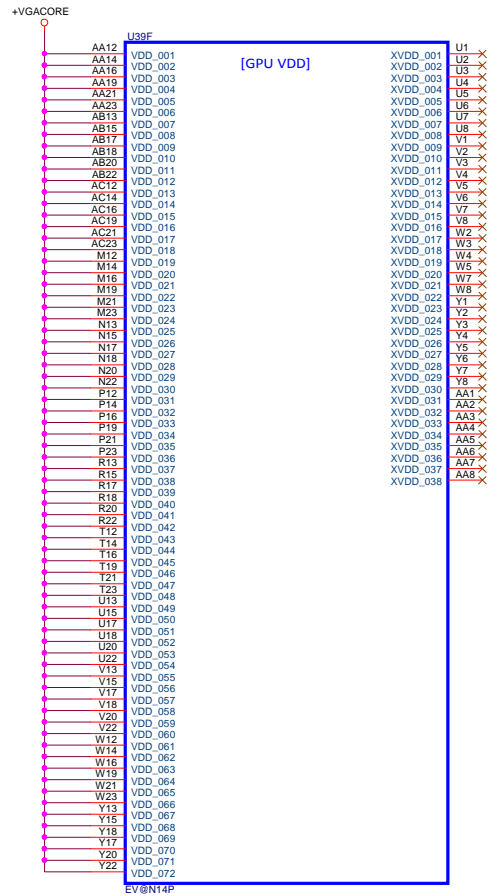
Table 9. N14P-GV/GT/GS/LP/GE GDDR5 Recommended Memories
128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Data Code Minimum	Status
128Mx16 GDDR5	Hynix	0x4	1.5 V/ 1.5 V	H5GQ2H24AFR-T2C	2500	N/A	Production Candidate
		0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	K4G20325FD-FC04	2500	1219	Production Candidate
		0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Production Candidate

Vendor	P/N	Mfr. P/N	ROM_S
Hynix	AKG5MMUTW13	H5GQ2H24AFR-T2C	0100
Samsung		K4G20325FD-FC04	0101

SMBus(VGA)



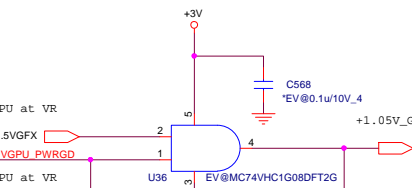


for meet Power down sequence
for +3V_GFX

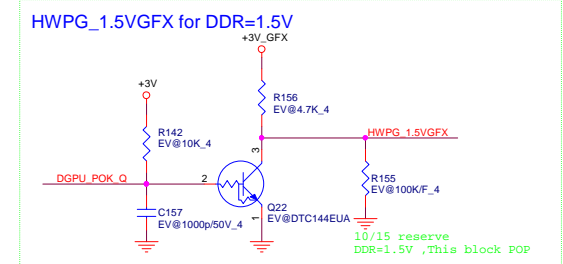
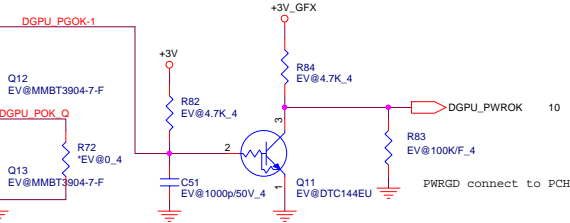
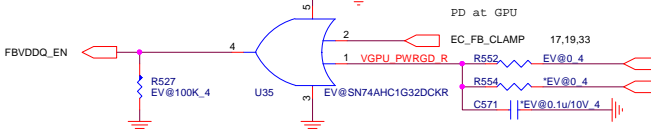
+VGACORE → D14 → EV@RB500V-40 → +3V_GFX

+1.5V_GFX → D13 → "EV@RB500V-40 → +3V_GFX

No stuff when GC6 support.



GC6 need system 3V to control FBVDDQ



CHANNEL A: 1024MB DDR3X16

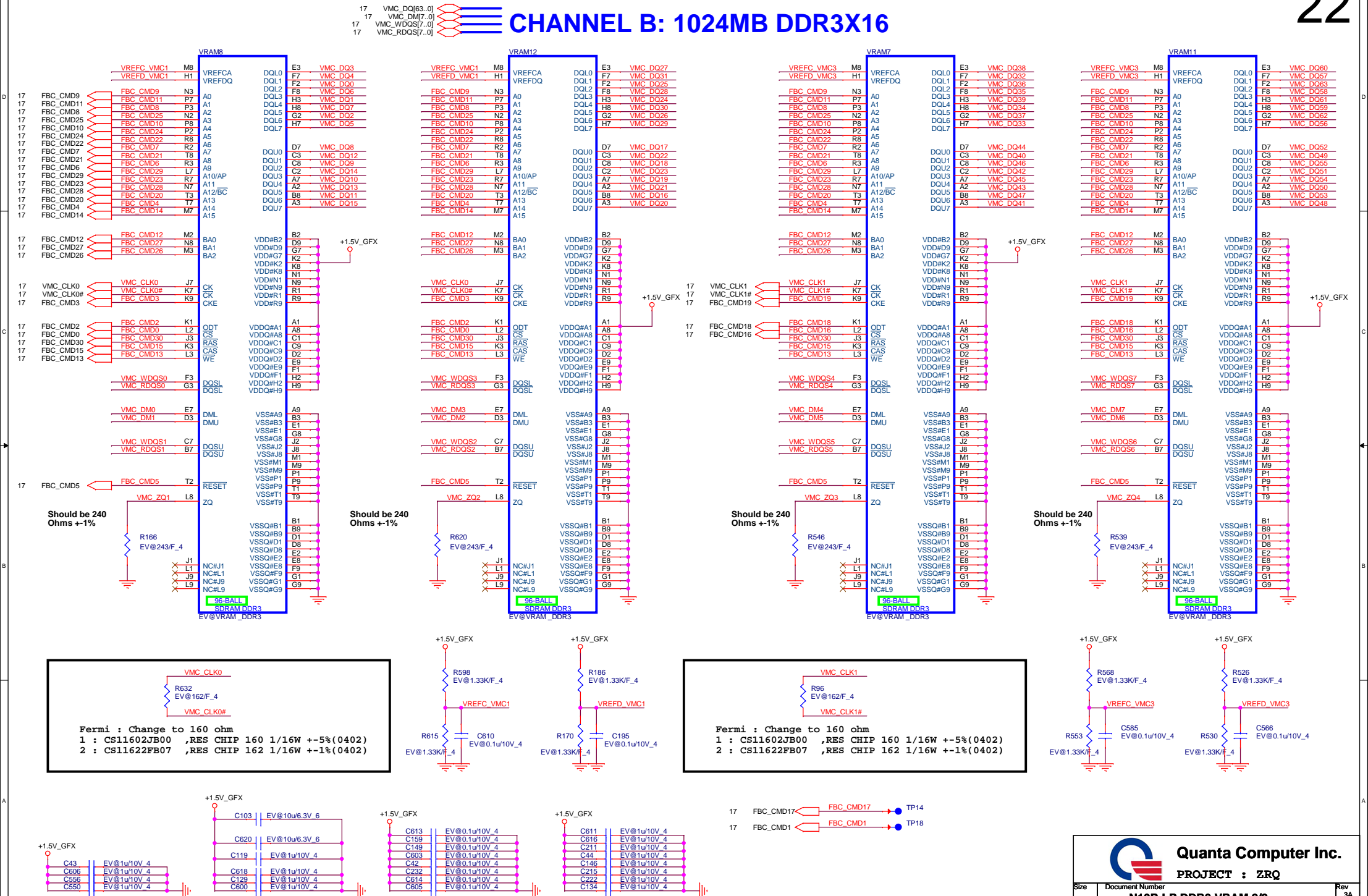
**Quanta Computer Inc.**

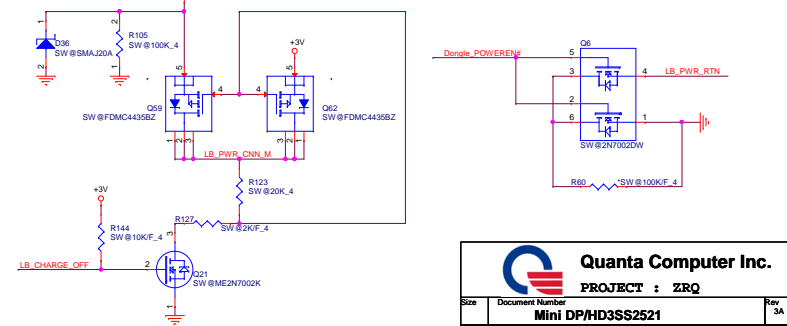
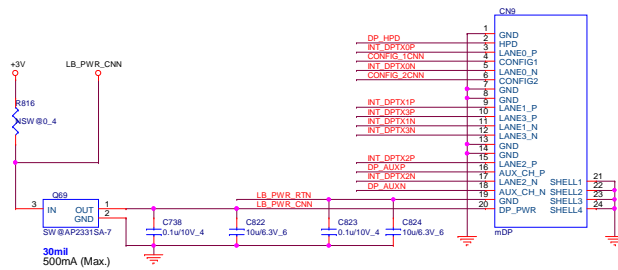
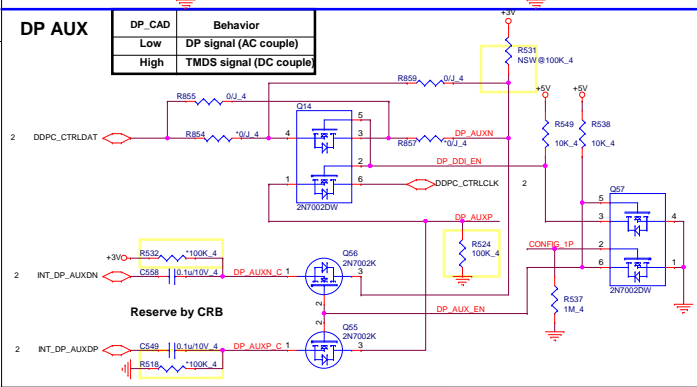
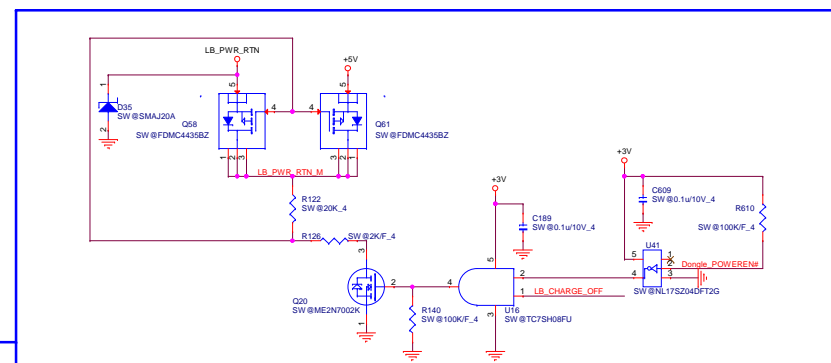
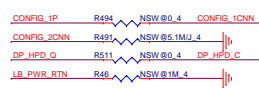
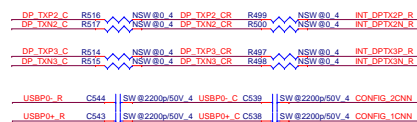
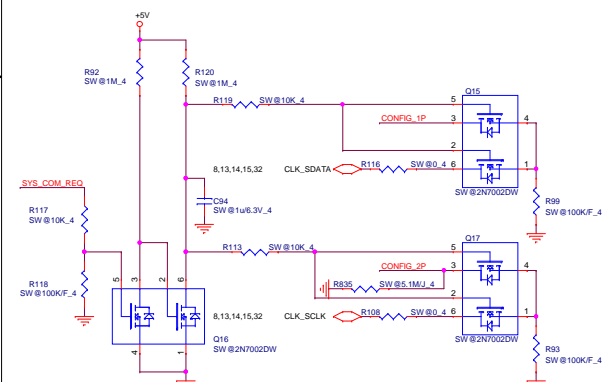
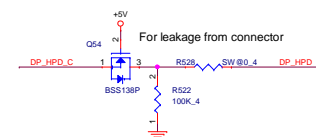
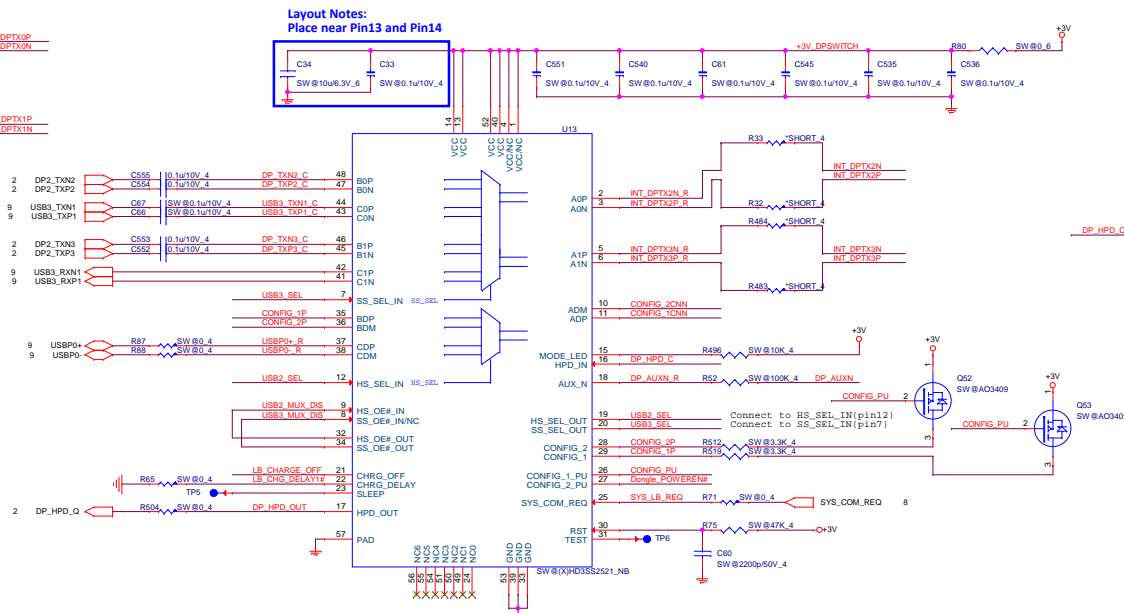
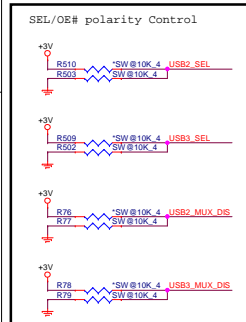
PROJECT : ZRQ

Size	Document Number
	NN13P-LP DDR3 VRAM 1/2

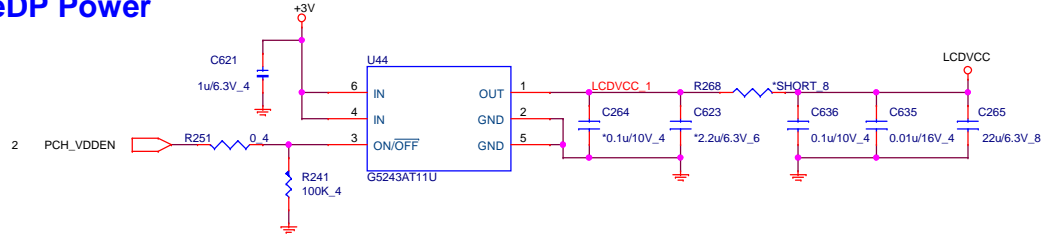
Rev
3A

CHANNEL B: 1024MB DDR3X16

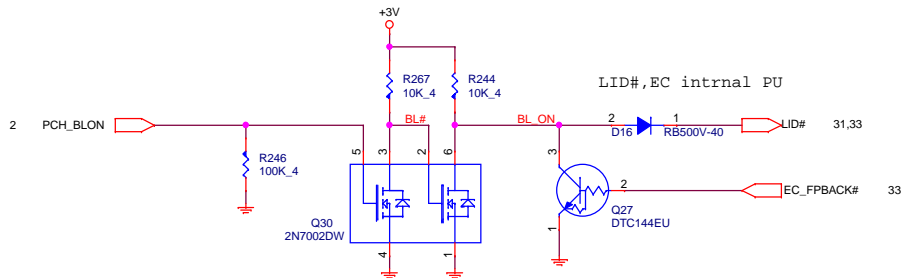




eDP Power



Backlight Control



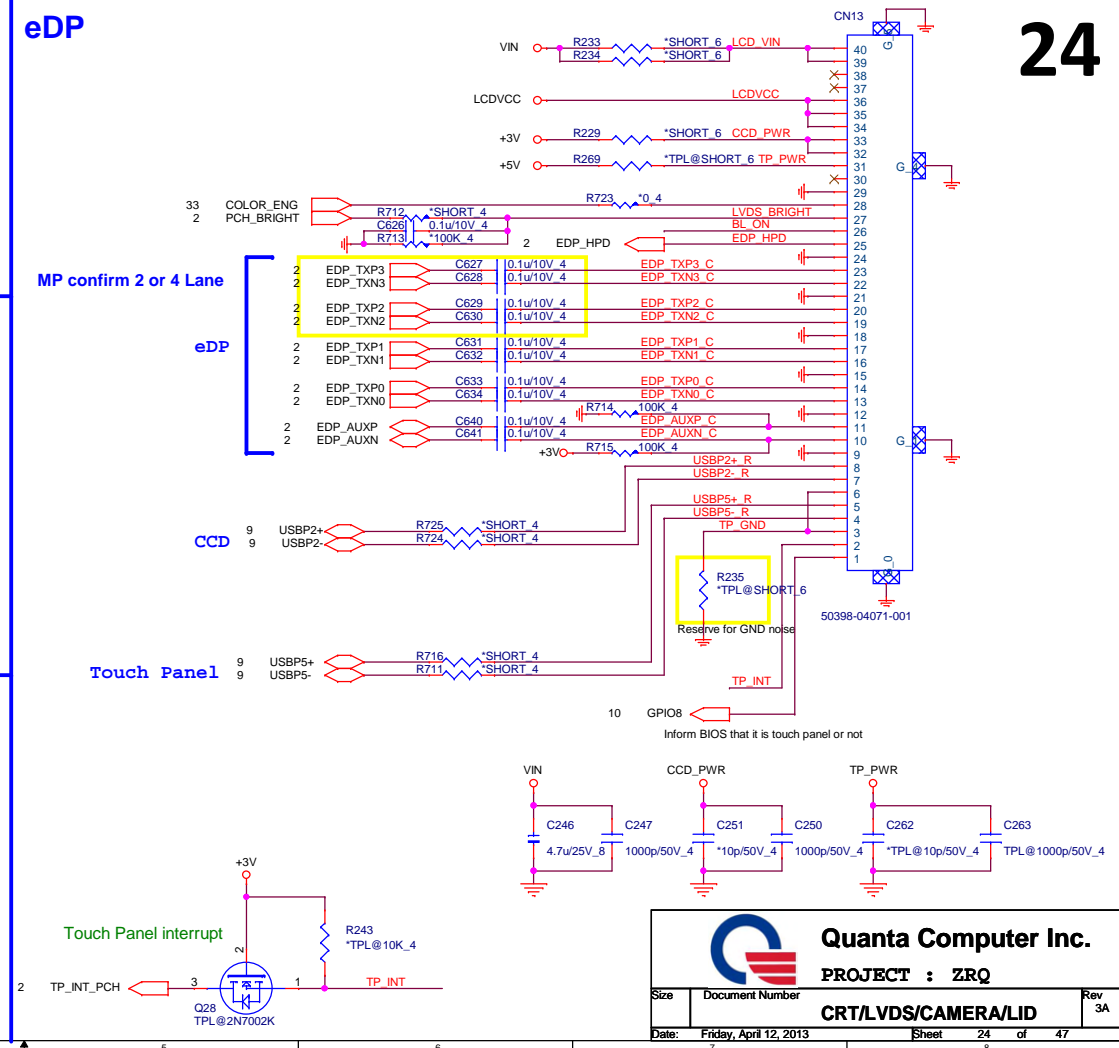
Lid Switch (HSR)(move to USB/B)

eDP

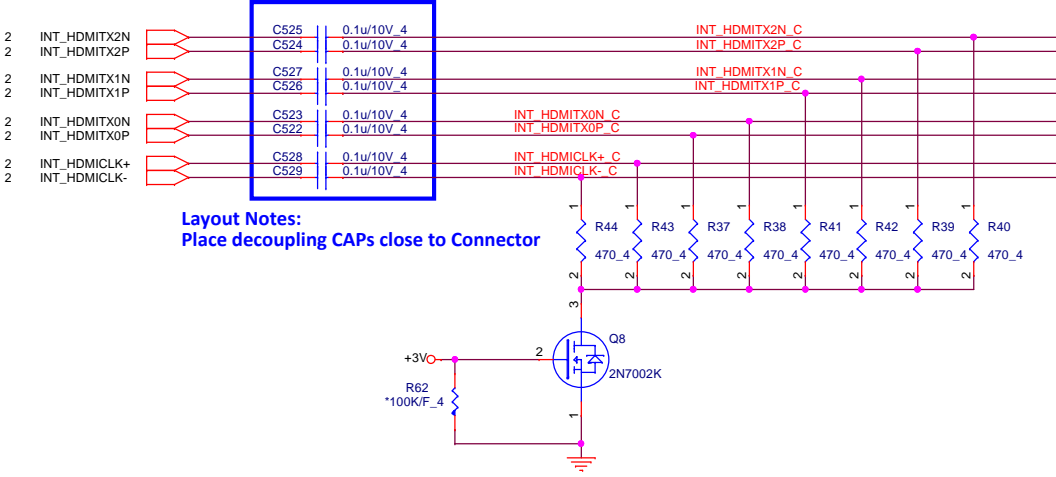
MP confirm 2 or 4 Lane

eDP

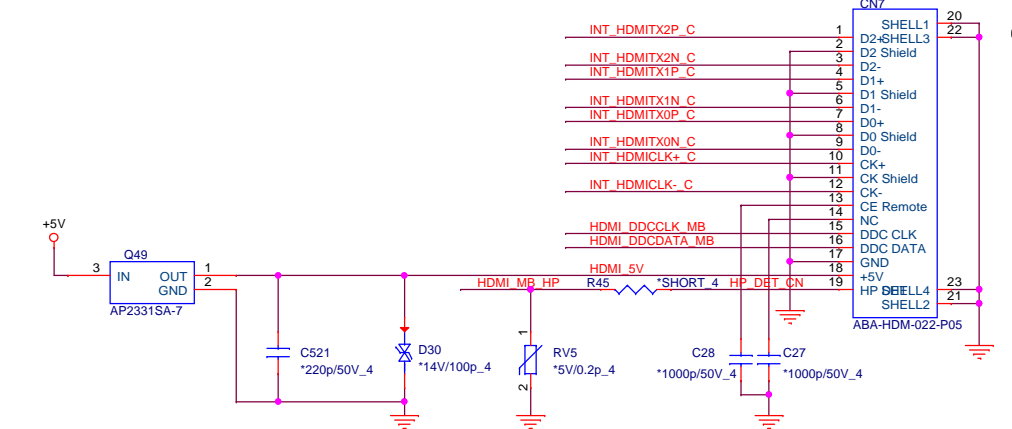
Touch Panel



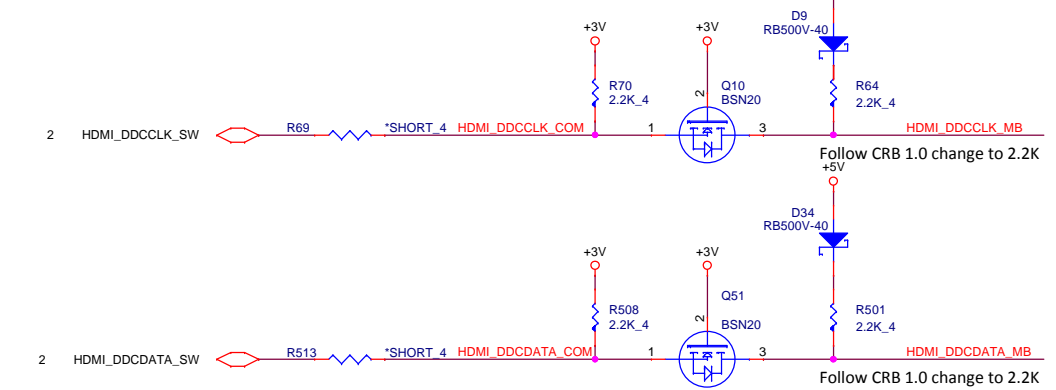
HDMI Cost Reduced level shift (HDM)



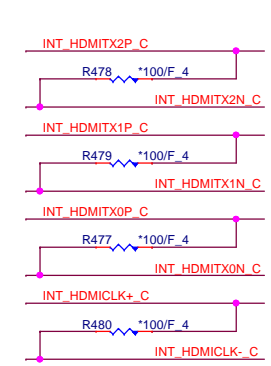
HDMI connector (HDM)



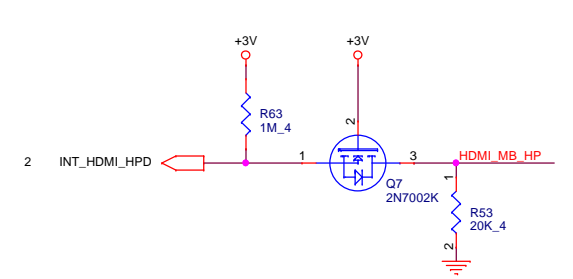
HDMI DDC (HDM)



EMI (EMC)



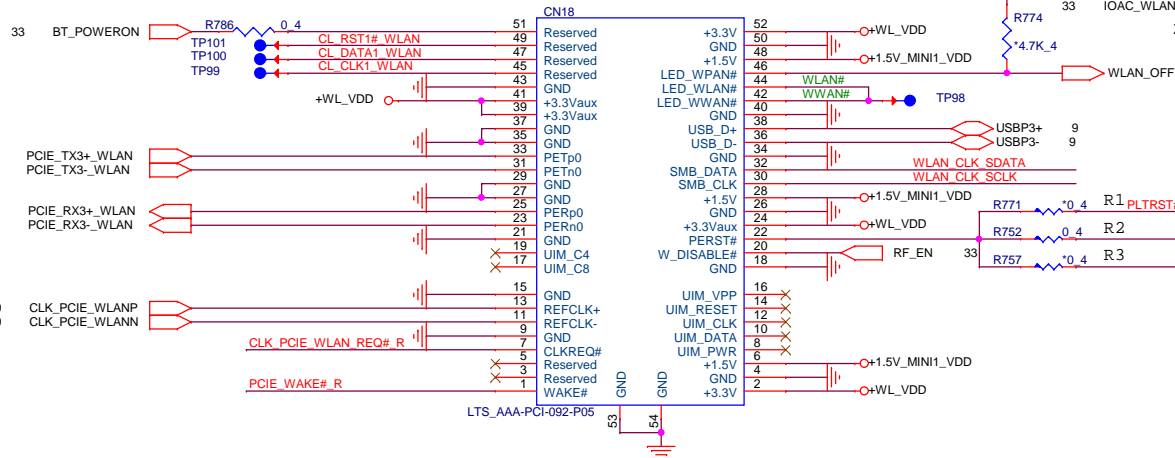
HDMI-detect (HDM)



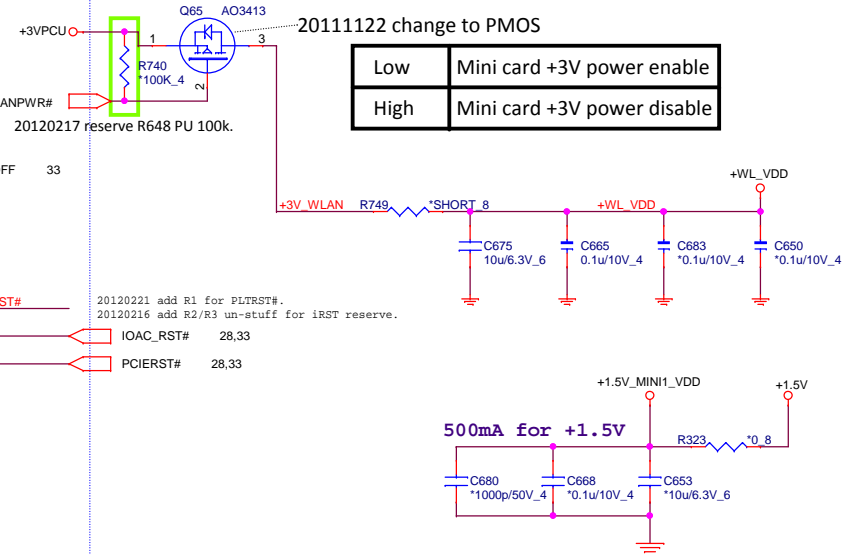
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)
H=5.2mm



2011017 : stuff Q81 to enable wake function on WLAN for IOAC
check IOAC power rail can reduce Q81

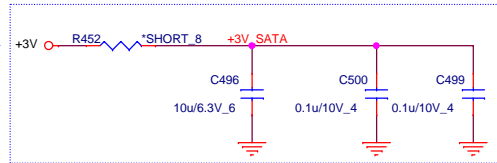


LAYOUT NOTE:
CLOSE TO CONNECTOR

mSATA(MNC)

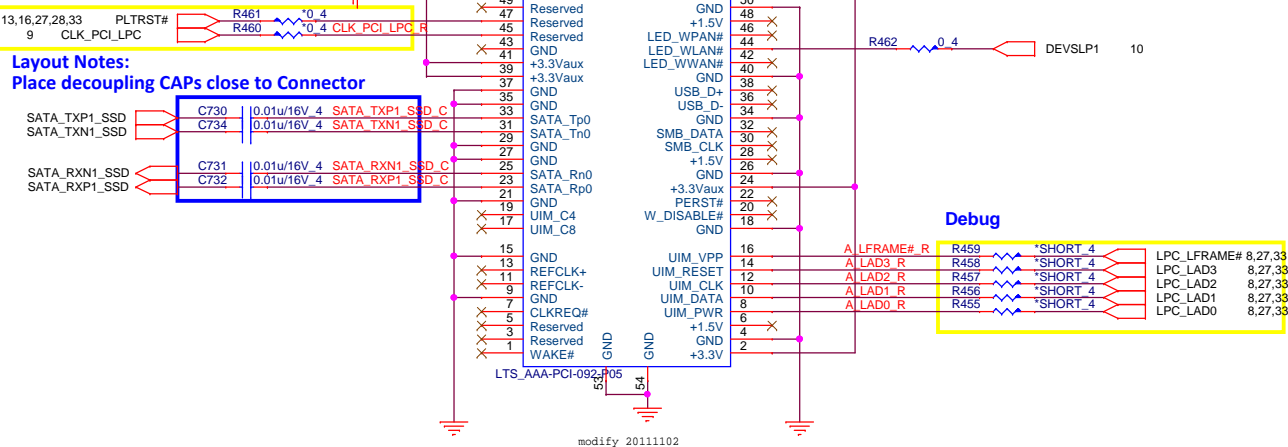
LAYOUT NOTE:
CLOSE TO CONNECTOR

rating = 1000mA @ 128G



H=4.95mm

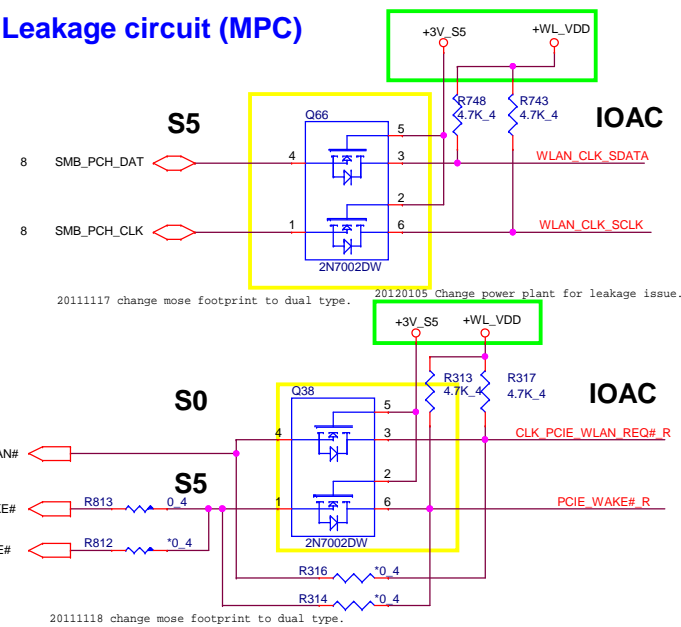
Debug




modify 20111102

Leakage circuit (MPC)

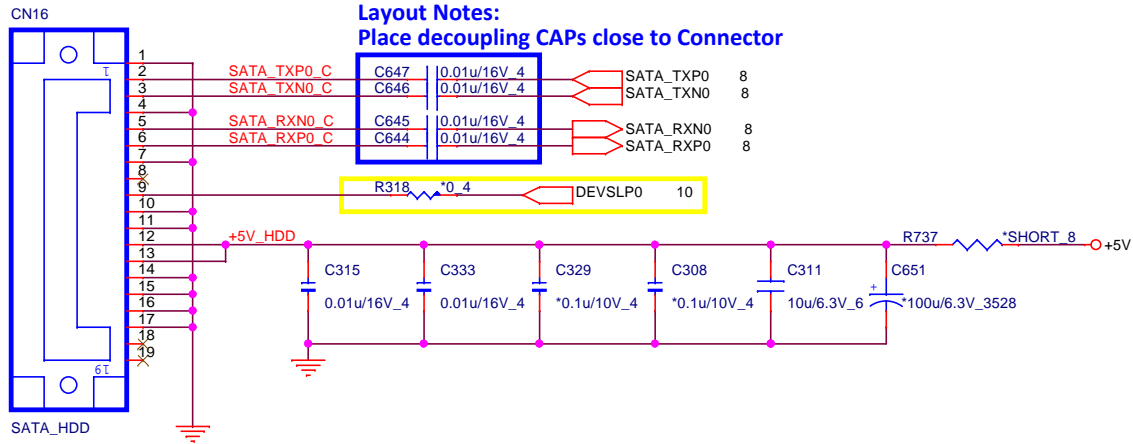
20120105 Change power plant for leakage issue.



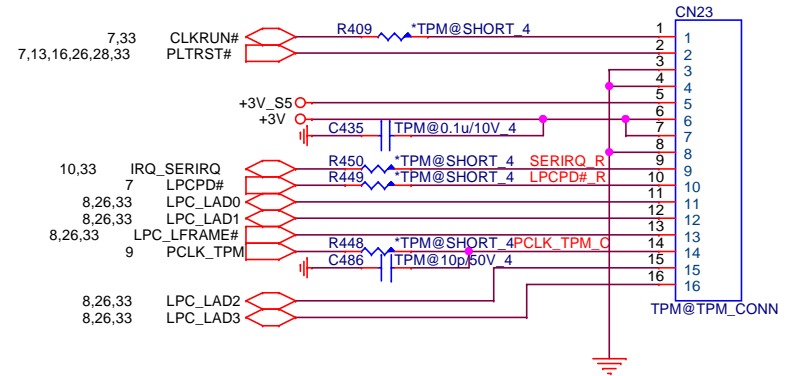
20111118 change mose footprint to dual type.

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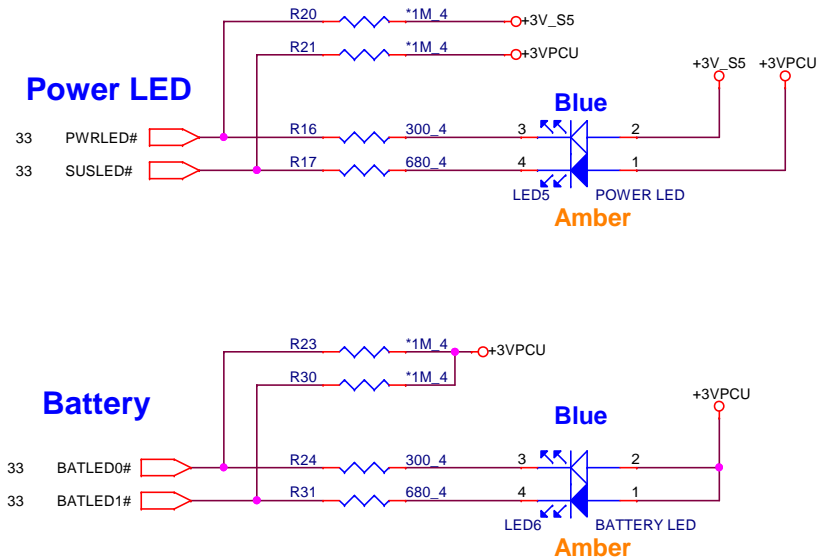
MAIN SATA HDD (HDD)



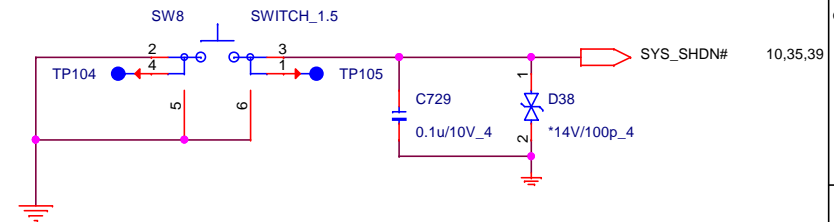
TPM (TPM)



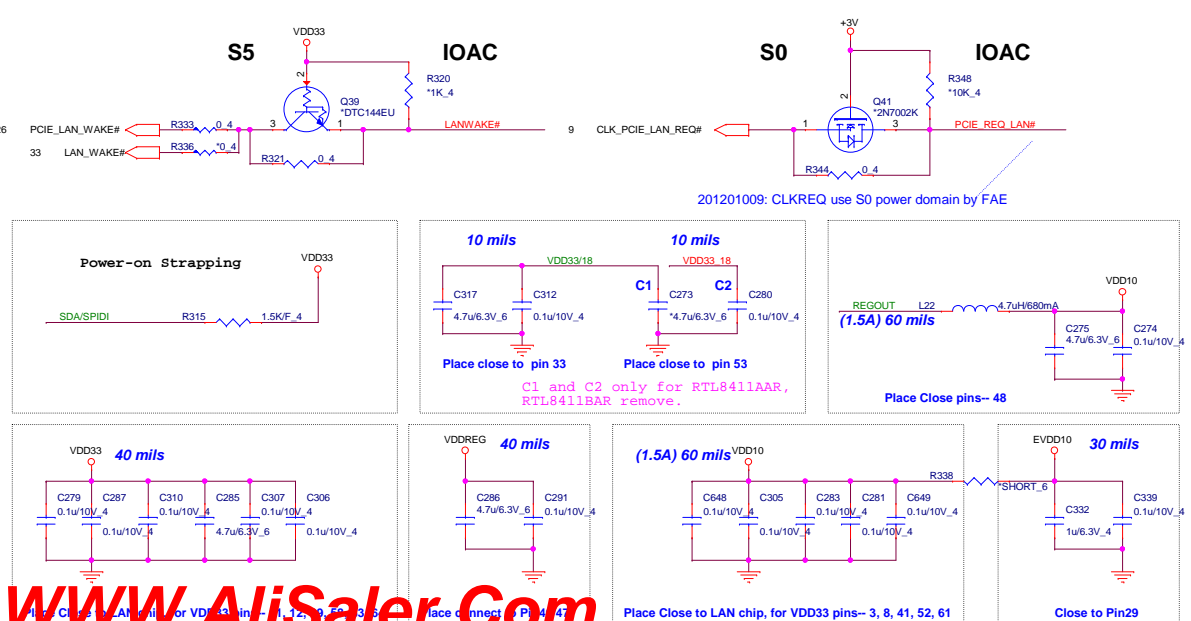
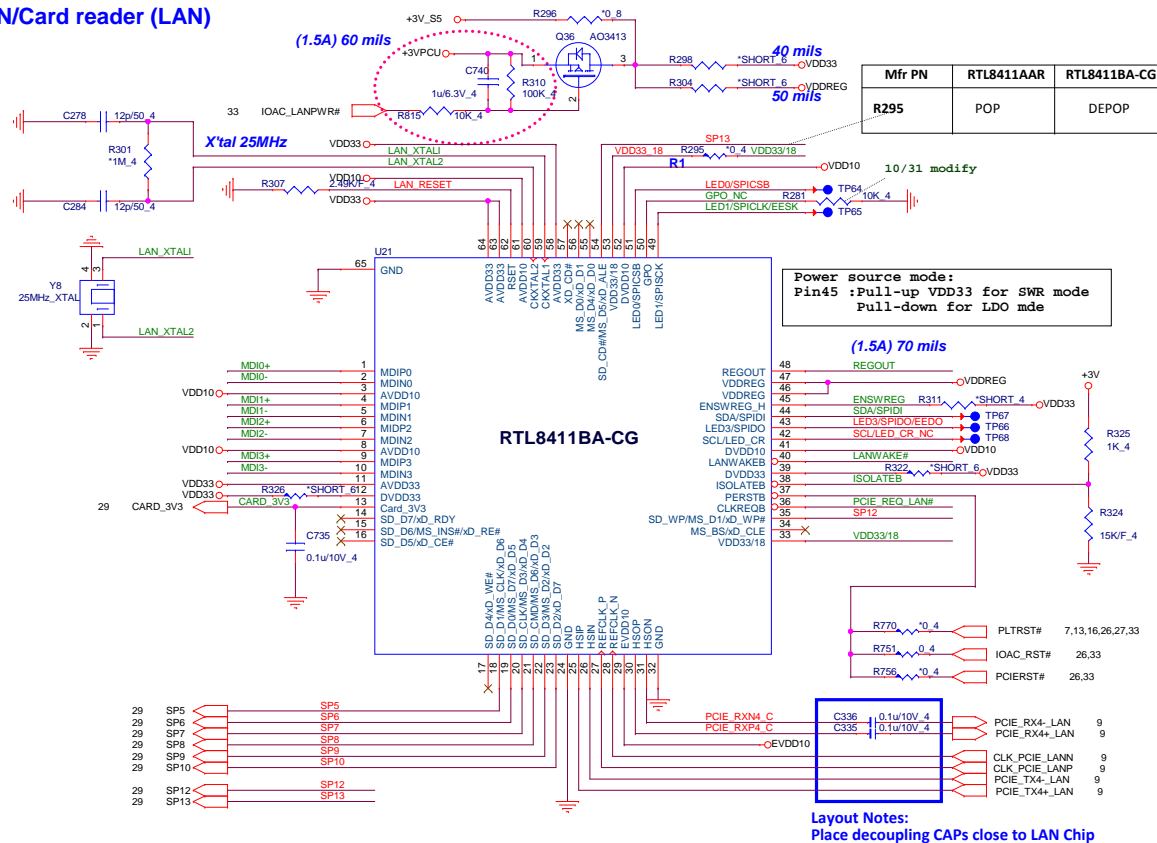
LED(UIF)



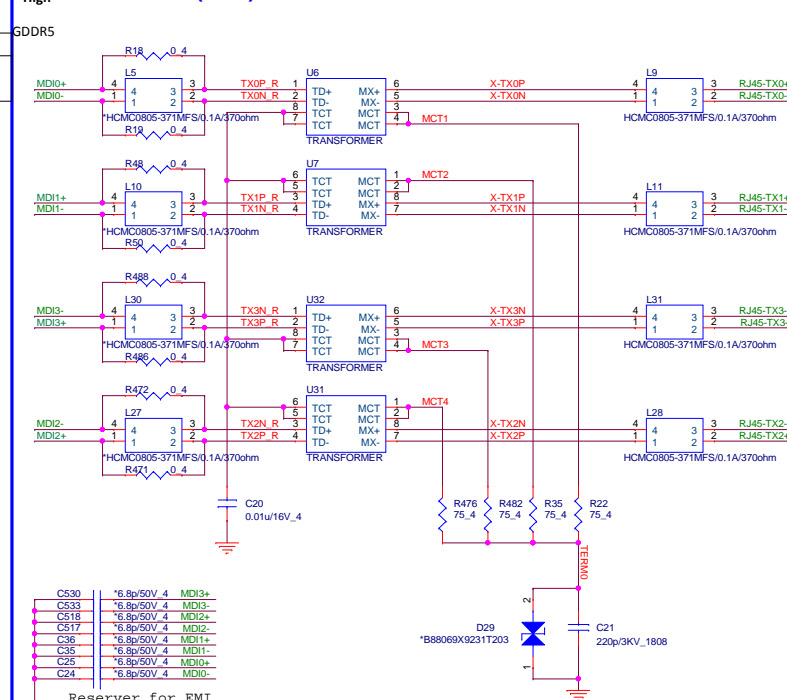
3/5VPCU reset switch (CLG)



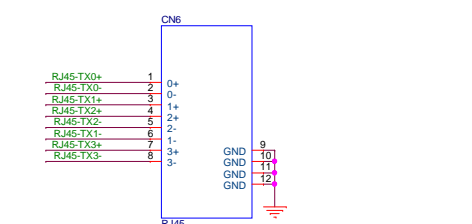
LAN/Card reader (LAN)



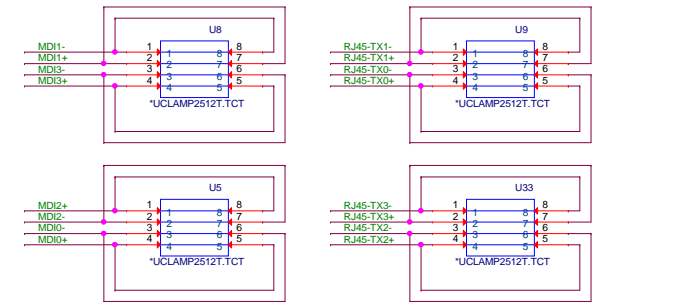
High Transformer (LAN)



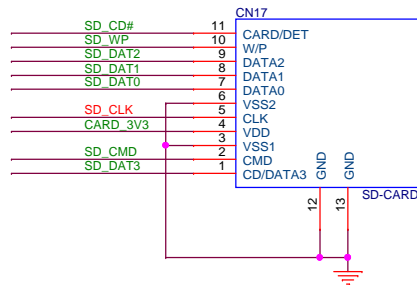
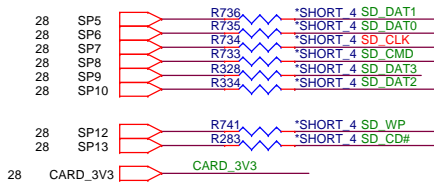
RJ45 CONNECTOR (LAN)



SURGE (LAN)



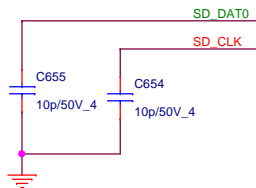
SD/MMC CARD READER CONNECTOR (MMC)



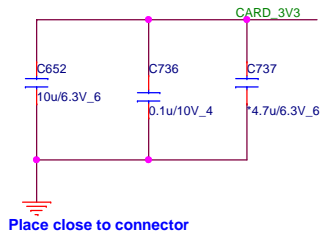
EMI

Share Pin

SP1	SD D7	xD RDY
SP2	SD D6	MS_INS#
SP3	SD D5	xD_RE#
SP4	SD D4	xD_CE#
SP5	SD D3	xD_WE#
SP6	SD D2	xD_D6
SP7	SD D1	MS_CLK
SP8	SD D0	xD_D5
SP9	SD D7	MS_D3
SP10	SD D6	xD_D4
SP11	SD D5	MS_D6
SP12	SD D4	xD_D3
SP13	SD D3	MS_D2
SP14	SD D2	xD_D2
SP15	SD D1	xD_D7
SP16	SD D0	MS_BS
SP17	SD WP	xD_CLE
SP18	SD CD#	MS_D1
SP19	MS D5	xD_WP#
SP20	MS D4	xD_ALE
SP21	MS D3	xD_D0
SP22	MS D2	xD_D1
SP23	MS D1	xD_CD#
SP24	MS D0	

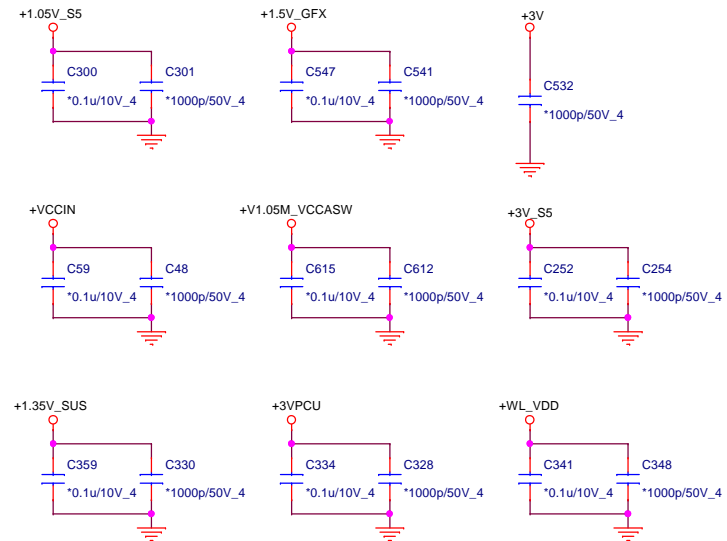


10 mils

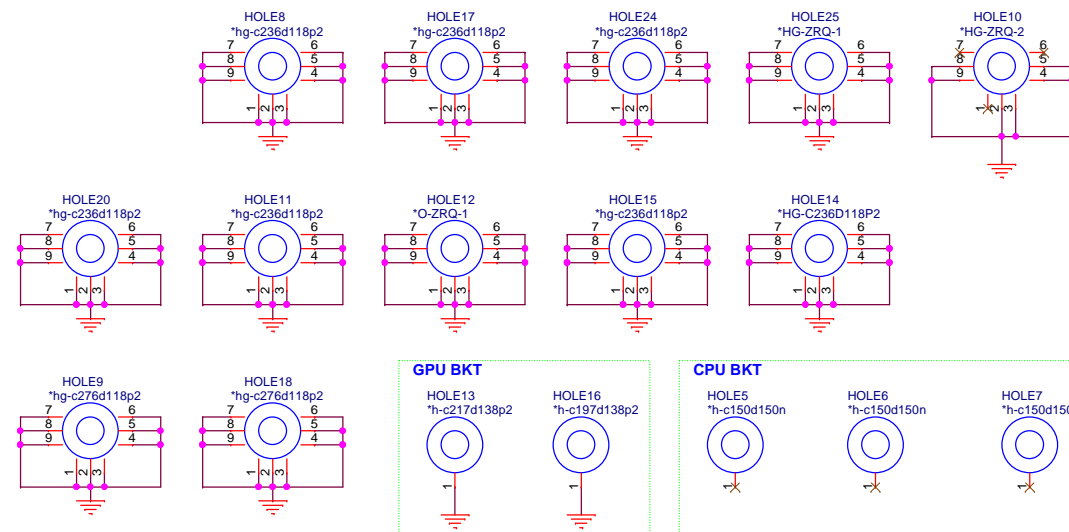


Stitching cap (EMC)

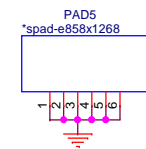
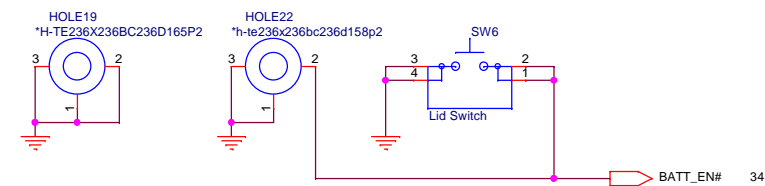
29



HOLE(OTH)

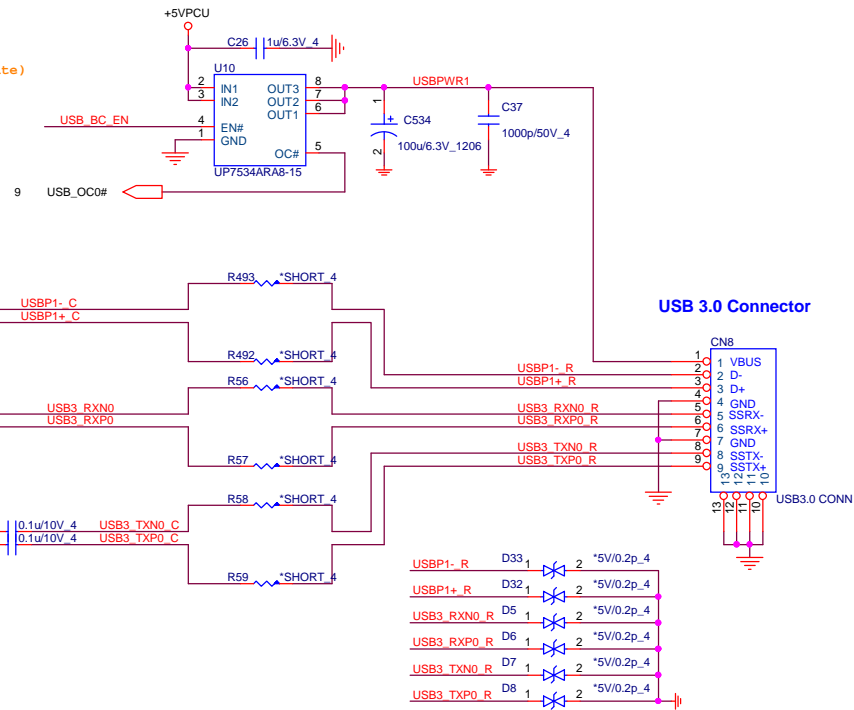


BATT Enable short pad



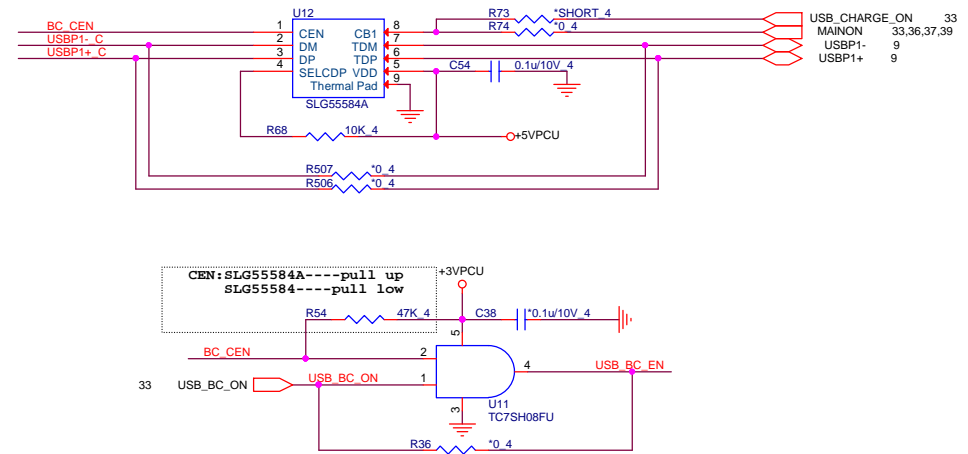
USB3.0

Active High:
1st: AL007534001 (Promote)
2nd: AL000547006 (GMT)
3rd: AL002511002 (DDS)

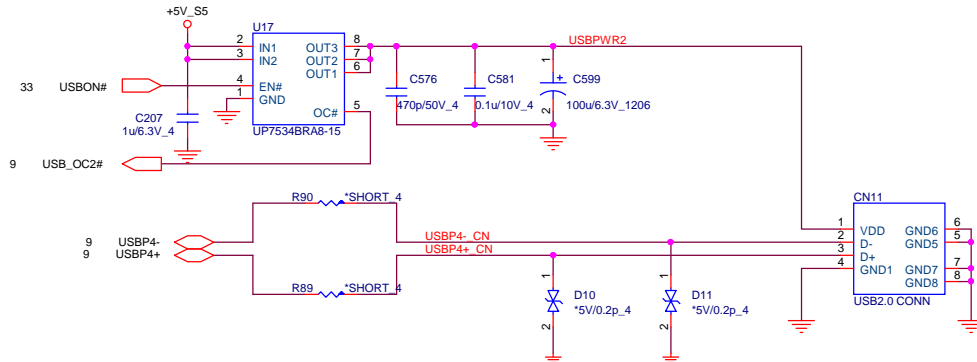


USB Charger to 3.0

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDF only
1	1	S0 charging with CDP or SDF only (depending on external device)

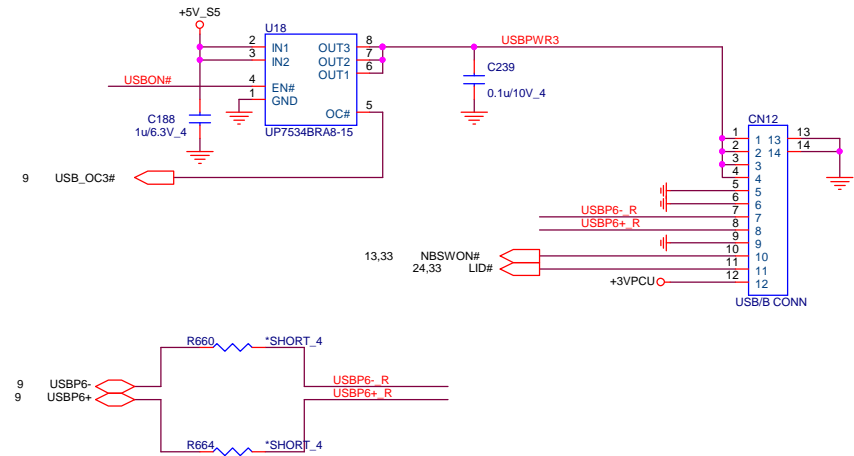


USB2.0



I/O board

1st source: AL007534000
2ns source: AL082025000

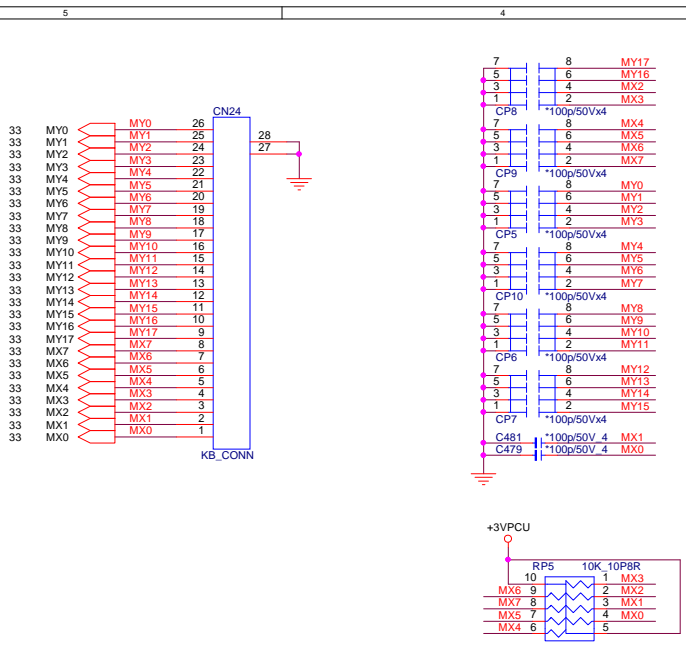


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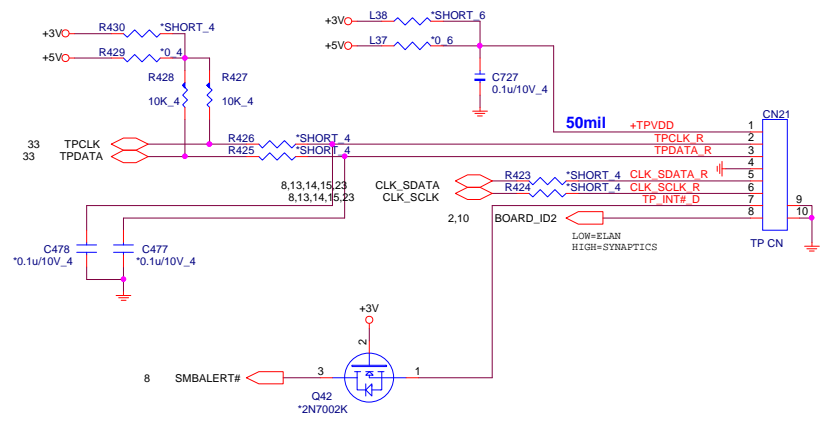
PROJECT : ZRQ

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	INT&EXT USB	3A
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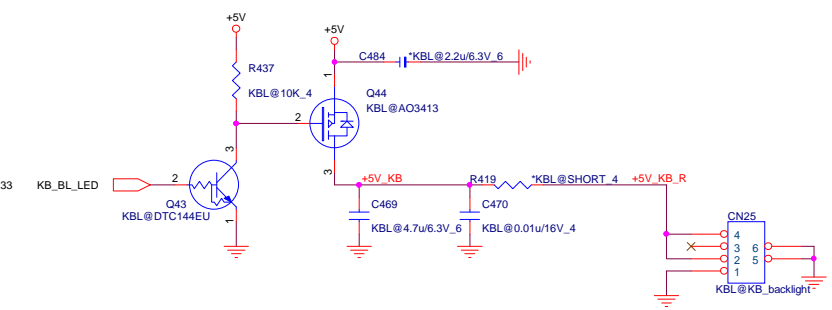
K/B (KBC)



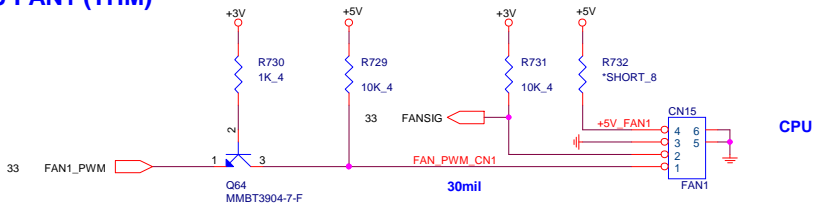
TOUCHPAD BOARD CONN (TPD)



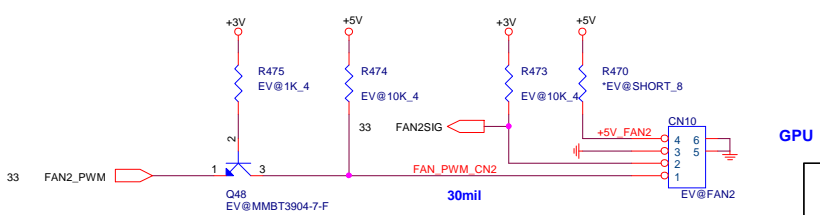
KB_BL LED (KBC)



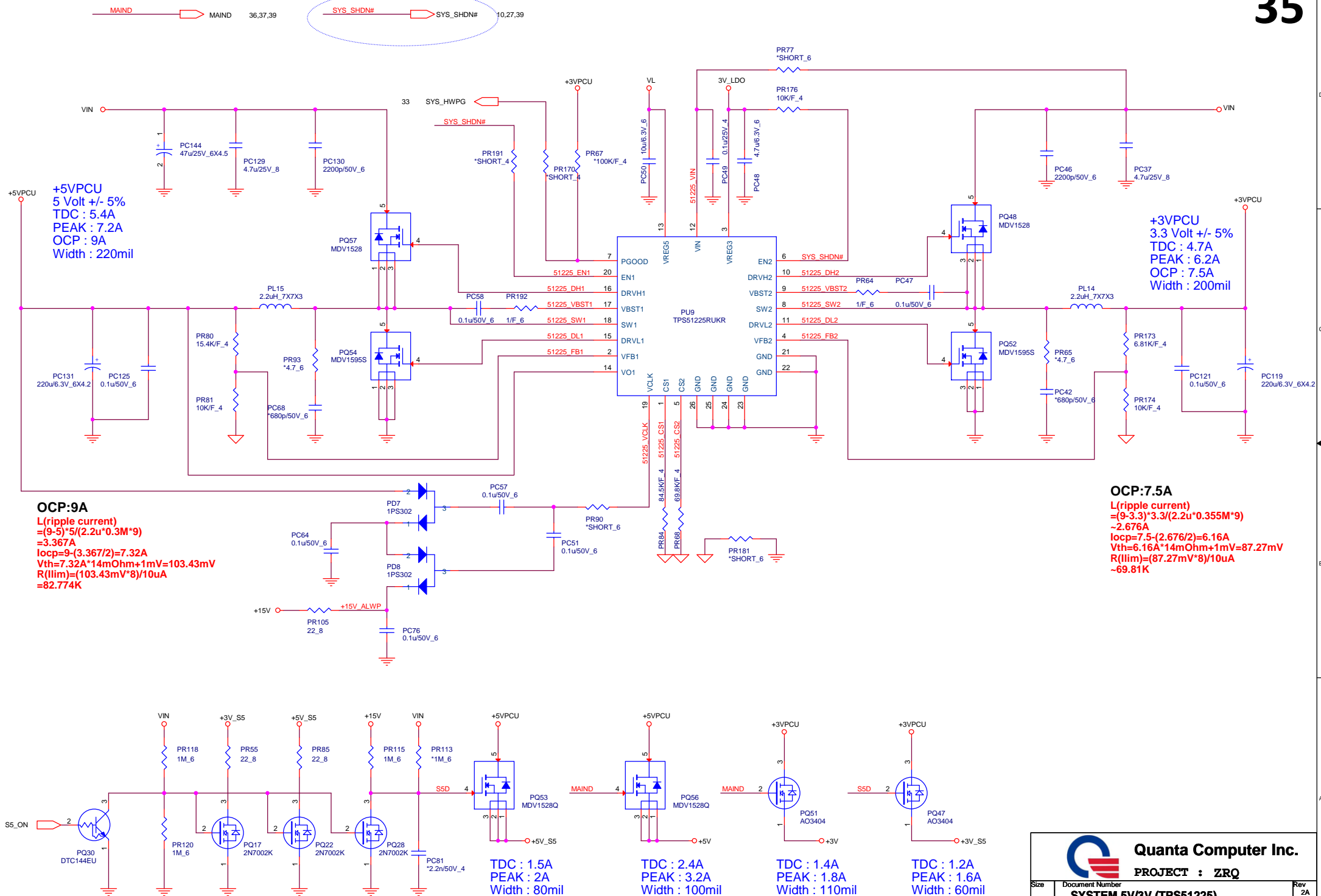
CPU FAN1 (THM)

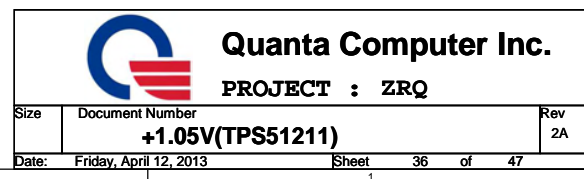
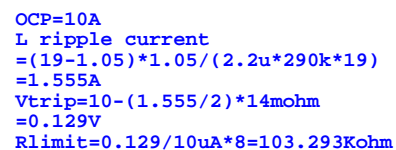


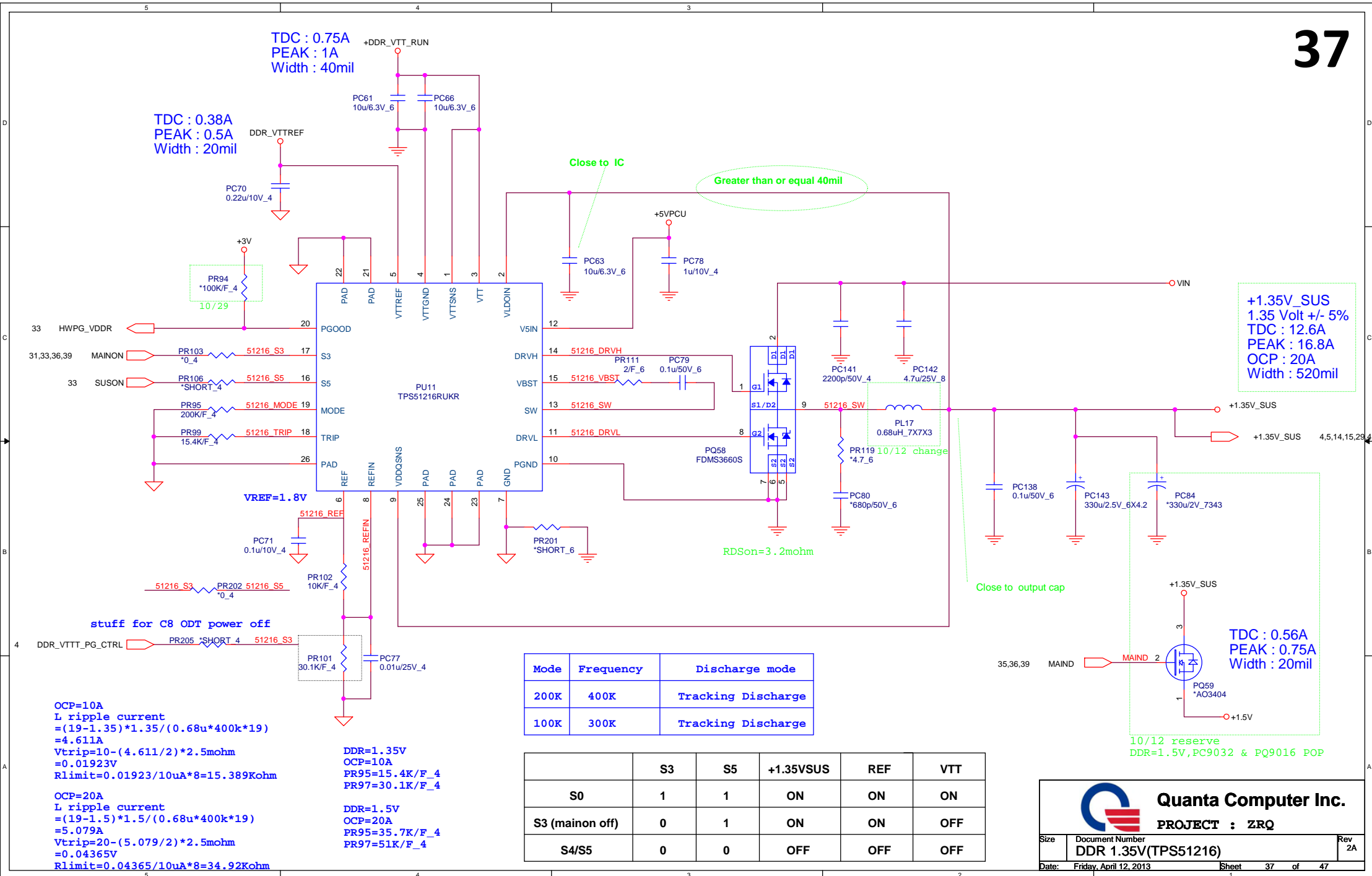
CPU FAN2 (THM)



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KB/TP/FAN
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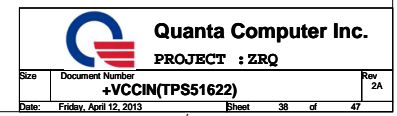




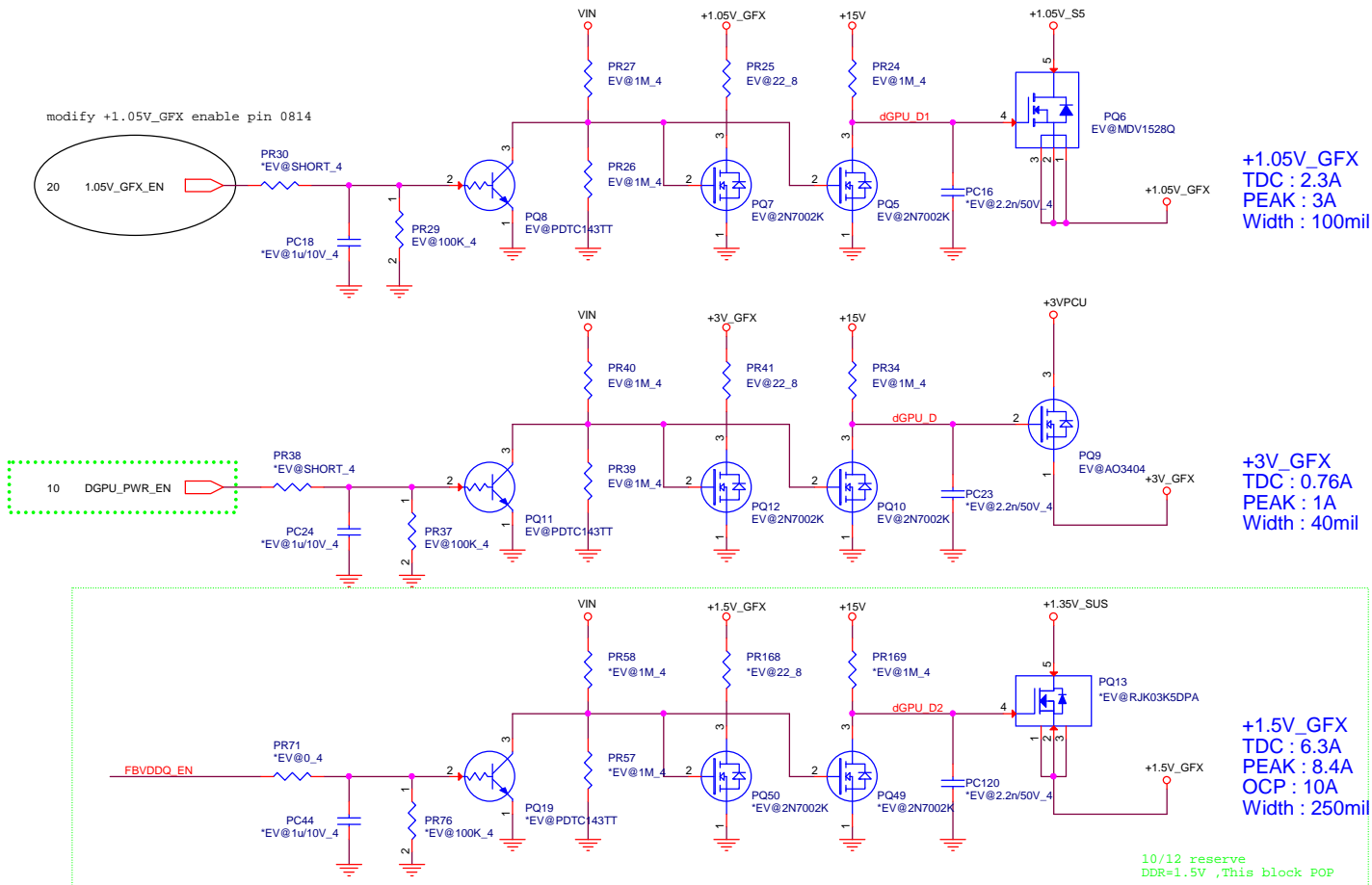
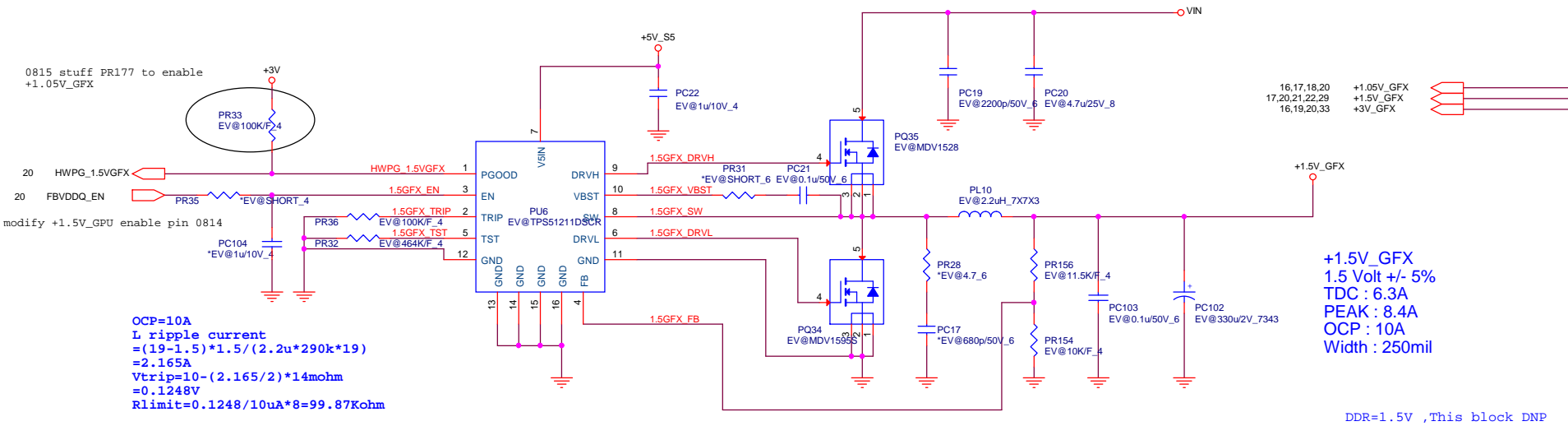
Quanta Computer Inc.

PROJECT : ZRQ

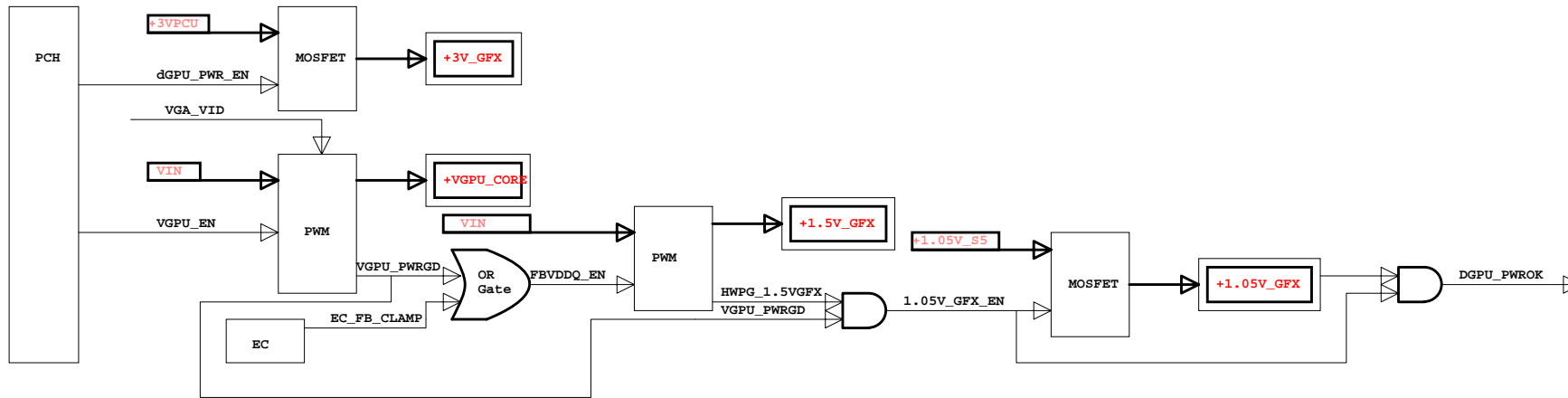
Size	Document Number	Rev
	DDR 1.35V(TPS51216)	2A
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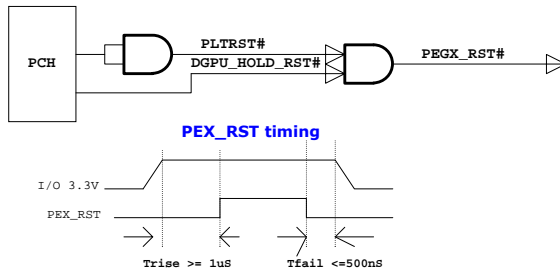




VGA power up sequence



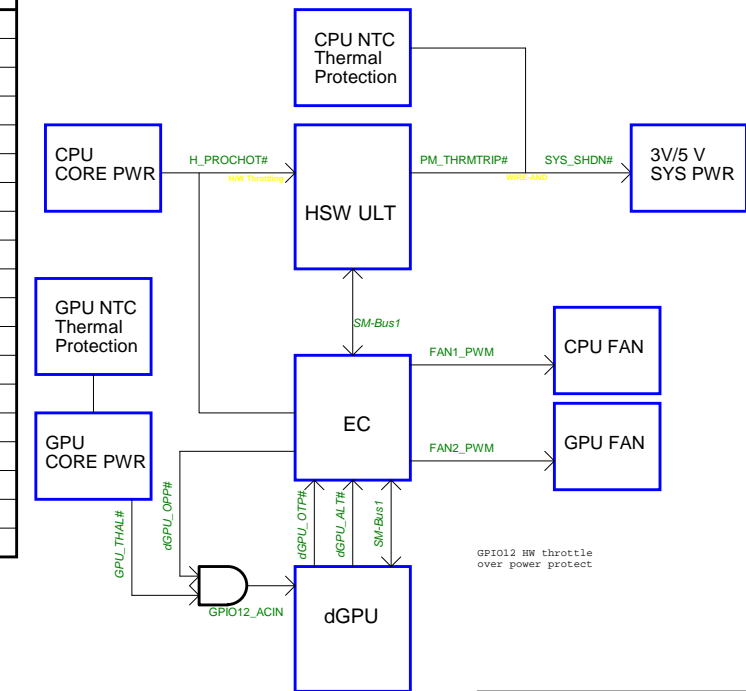
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+VGPU_CORE	variation	External GPU POWER	VGPU_EN	S0
+3V_GFX	+3.3V	External GPU POWER	dGPU_PWR_EN	S0
+1.5V_GFX	+1.5V	External GPU POWER	FBVDDQ_EN	S0
+1.05V_GFX	+1.05V	External GPU POWER	1.05V_GFX_EN	S0

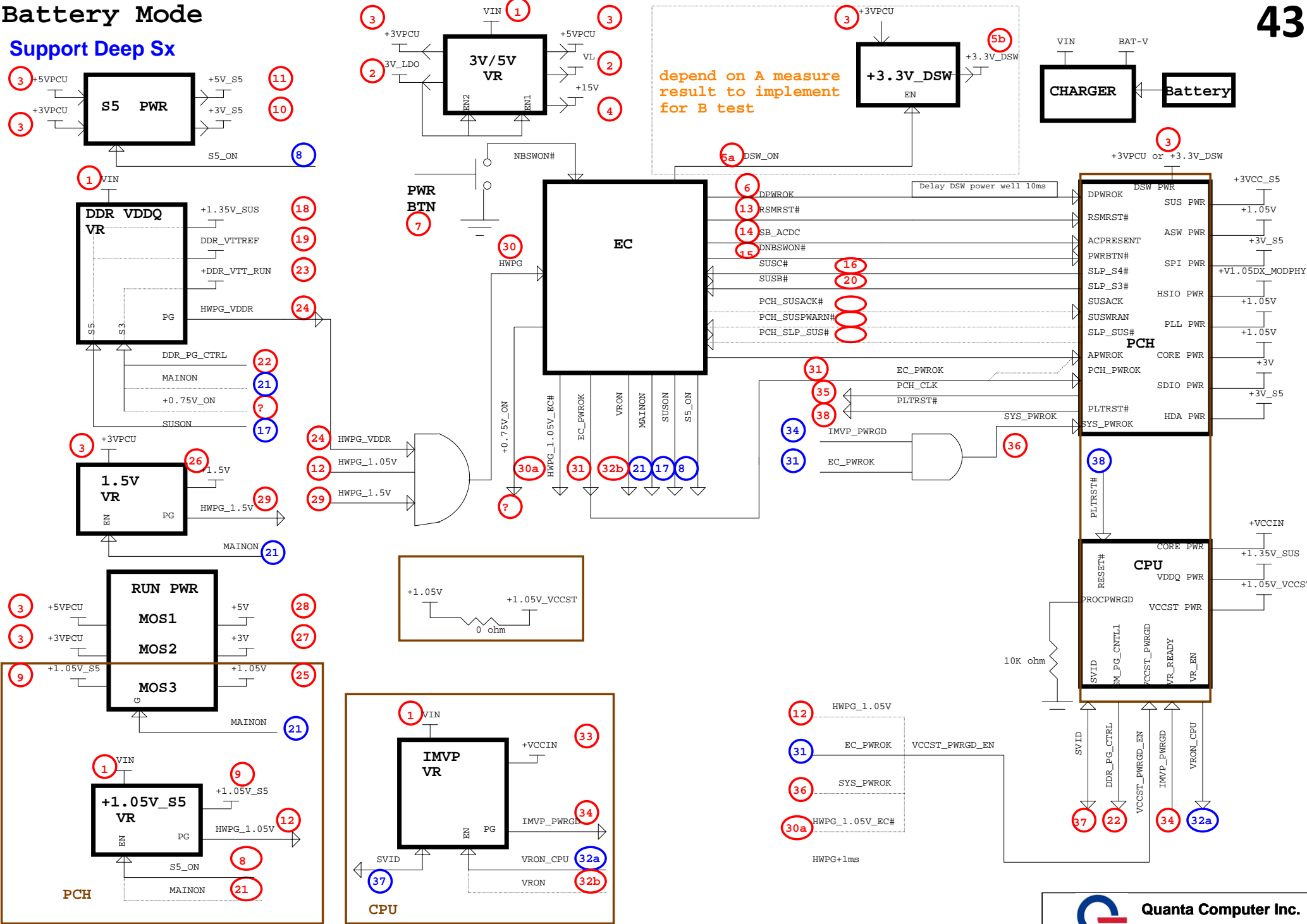
Thermal Follow Chart

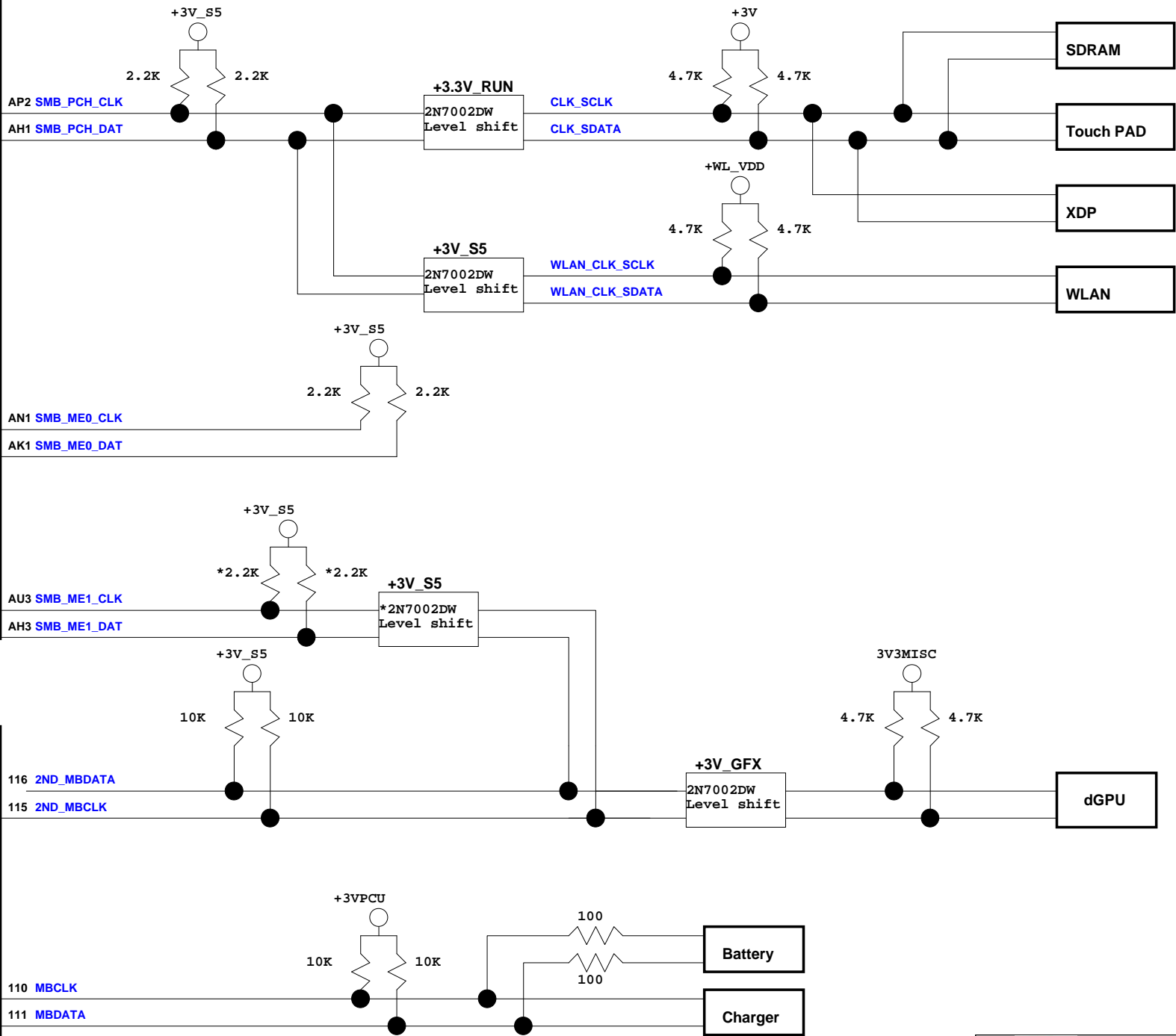
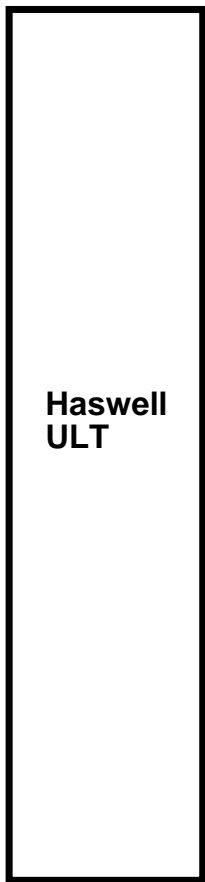


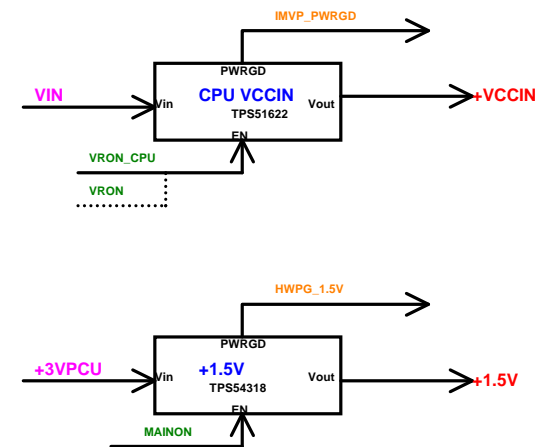
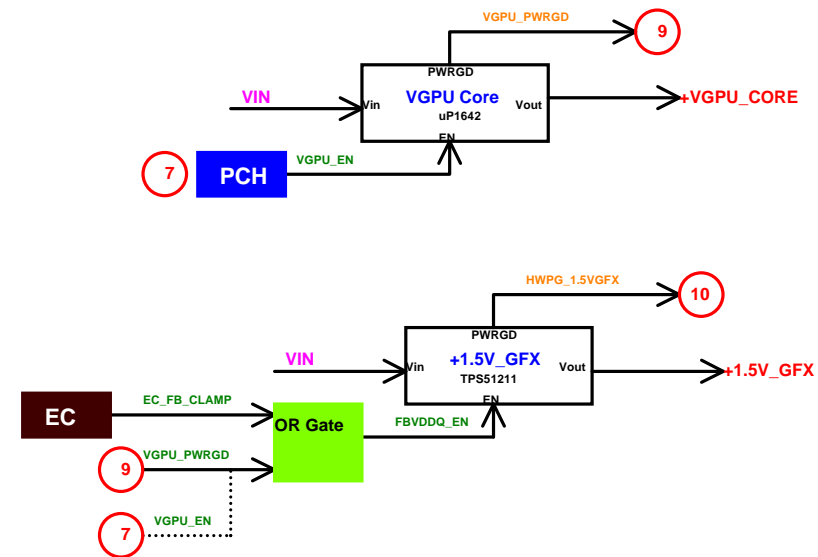
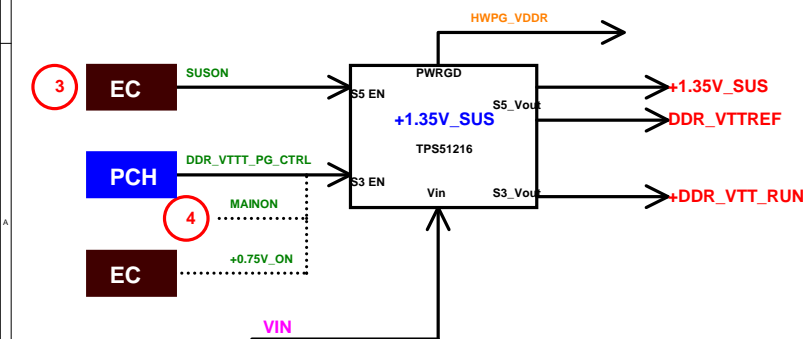
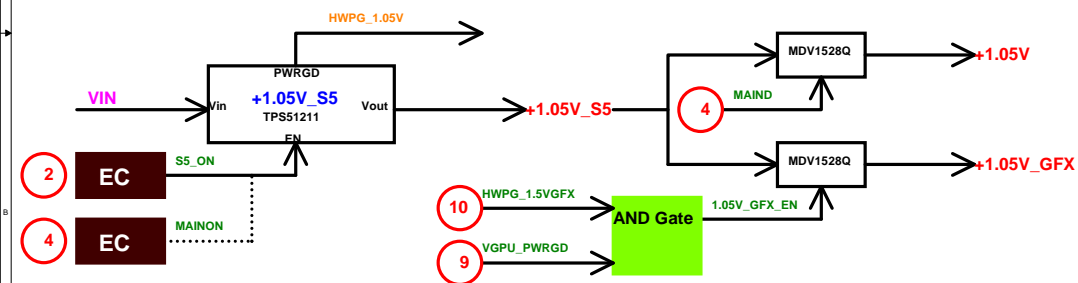
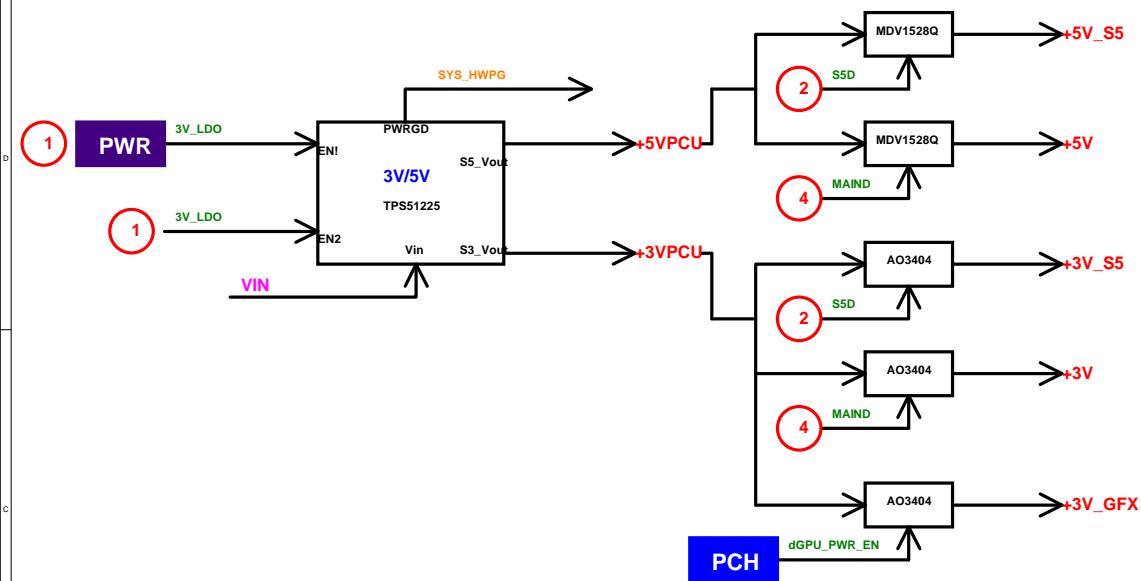
```
dGPU_OPP# EC notify HW throttle over power protect
dGPU_ALT# for ADPS circuit to inform EC NV dGPU VPS Alert
dGPU_OTP# VGA thrmtrip# => inform EC over temperature protect
```

Battery Mode


Support Deep Sx







DOC NO. PROJECT MODEL ZRQ APPROVED BY: DATE: **WWW.AliSaler.Com**

Model	Version	CHANGE LIST				
ZRQ	3B	<div>1 R276 change fro to 10K to 1K ,Depop R328.(PCIE_LAN_WAKE#),内部行文</div> <div>2 Change C24 KB Conn FN to DFFC26F083 .(Page 32),内部行文</div> <div>3 Change U27 EC to E version A108S870F95 .(Page 33),内部行文</div> <div>4 Fine tune Amp Gain =>R422,R411 change from 0 ohm to 1k , and pop R421,R410 to 1.62K .(Page 30)</div> <div>5 Change TEMP_MBAT from Pin 6 to Pin 5 of PJJ .(Page 34)</div> <div>6 Depop Q24 , and Add R228 to solve level abnormal issue for CG6 .(Page 19)</div> <div>7 Add RS16 and net "LB_PWR_CNN_Q" to stuff Q69 always for safety issue .(Page 19)</div> <div>8 Reserve R855,R859 and add R854,R857 .(Page 23)</div> <div>9 For WHQL Change USB Port1 and Port4</div> <div>10 Add new on Board RAM HYNIX H5TC4G6A9FR-PB1A RAM ID:0000</div> <div>11 Del L353,363,63,73,83,293,123,133,323,163,34</div>				
	3C	<div>1 Change to 0402 shortpad: R725,R724,R711,R716,R26,R27,R28,R29,R32,R33,R483,R484,R493,R492,R56,R57,R58,R59,R90,R89,R669,R664,R702,R638,R639,R651,R225,R346,R355,R779,R785,R790,R73 , R455,R456,R457,R458,R459,R343,R406,R396</div> <div>2 For HDMI 7-2 issue change R37,R38,R39,R40,R41,R42,R43,R44 To 470 ohm and remove R478,R479,R477,R480 (Page 25)</div> <div>3 For TI HD38S2521 issue R77,R79,R92,R503 need mount 10K, change R528 from 100 ohm to 0 ohm and remove R854,R857 , add R855,R859 .(Page 23)</div> <div>4 Change to 0603 shortpad: R373,R337,R382,R297,R235,R326,R322,L36,R385,R220,R254,R359</div>				
	3F	<div>1. Add C245 for intel request for G3 can't boot issue</div>				
DOC NO.	PROJECT MODEL	ZRQ	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISION:	
			<div><div>Quanta Computer Inc.</div><div>PROJECT : ZRQ</div><div>Change list-2</div></div>			